

RIYA Discrete Schematics Document

AMD Giffin CPU S1G2

VGA ATI M92S2-LP

RS780M + SB700

2009-08-25

REV : A00

DY : Nopop Component

TABLE OF CONTENTS

01_Cover Page	41_VREG : +VCC_GFX_CORE
02_Block Diagram	42_LCD&Inverter CONN
03_Power Block Diagram	43_(LAN&CRT CONN)
04_SMBUS BLOCK DIAGRAM	44_MiniCard&Card Reader CONN
05_THERMAL/AUDIO BLOCK DIAGRAM	45_HDD&ODD&FAN CONN
06_Table of Content	46_KeyBoard&TouchPad&BT CONN
07_Clock Generator ICS9LPRS480	47_USB CONN
08_CPU_HT_LINK I/F_(1/4)	48_EEPROM&LED&Camera&RTC CONN
09_CPU_DDR_(2/4)	49_Audio Jack
10_CPU_Control&Debug_(3/4)	50_IO BOARD CONN
11_CPU_Power_(4/4)	51_Express Card Board CONN
12_DDR_DIMM1	52_Power Button&Hall Sensor&MDC
13_DDR_DIMM2	53_Miscellaneous Components
14_ATi-RS780M_HT_LINK&PCie(1/4)	54_VGA-PCIE/LVDS(1/4)
15_ATi-RS780M_LVDS&CRT_(2/4)	55_VGA-TV/CRT/DP PORT(2/4)
16_ATi-RS780M_SidePort_(3/4)	56_VGA-POWER/GND(3/4)
17_ATi-RS780M_PWR&GD_(4/4)	57_VGA-MEMORY/STRAPS(4/4)
18_ATi-SB700_PCIE&PCI_(1/5)	58_VRAM
19_ATi-SB700_USB&GPIO_(2/5)	59_VRAM
20_ATi-SB700_SATA-IDE_(3/5)	60_CLOCK BLOCK DIAGRAM
21_ATi-SB700_POWER&GND_(4/5)	61_RESET BLOCK DIAGRAM
22_ATi-SB700_STRAPPING_(5/5)	62_POWER SEQUENCE
23_AUDIO CODEC IDT-92HD81	63_Change List-EE
24_(AUDIO AMP)	64_Change List-Power
25_Card Reader Realtek RTS5159	
26_LAN Realtek RTL8103EL	
27_KBC WPCE773L	
28_(Super I/O)	
29_THERMAL EMC2102	
30_Power On Logic	
31_Power Plane Enable	
32_DC IN/BATT CONN	
33_Charger MAX8731A	
34_VREG : +3.3V_ALW&+5V_ALW	
35_VREG : +VCC_CORE&+VDDNB	
36_(Reserve for Power)	
37_VREG : +1.1V_RUN	
38_VREG : +1.2V_RUN	
39_VREG : +1.8V_SUS&+0.9V_VTT	
40_VREG : +1.5V_RUN&+2.5V_RUN	


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Title Cover Page			
Size Custom	Document Number Riya Discrete		Rev A00
Date: Wednesday, August 26, 2009		Sheet 1	of 65

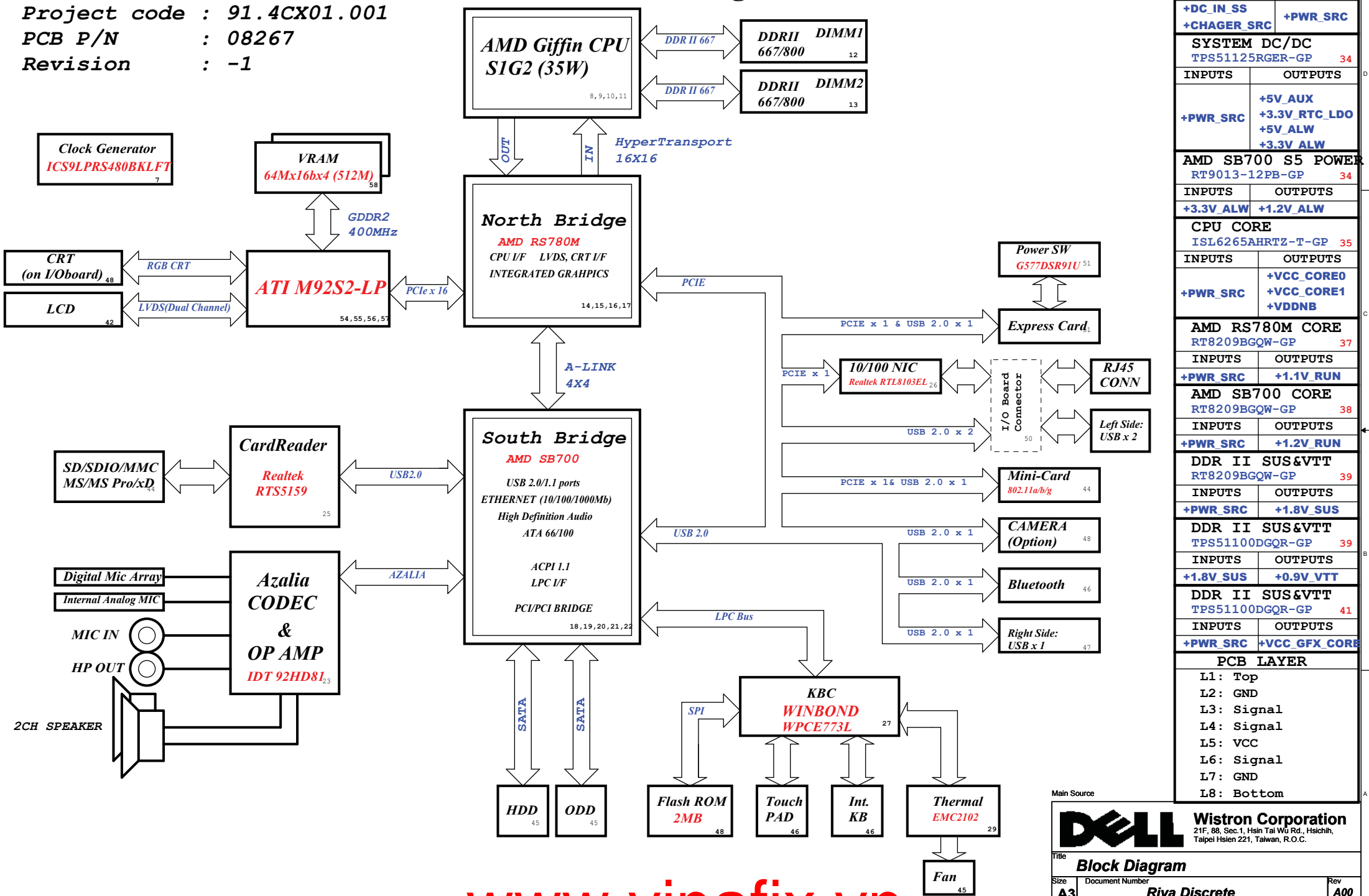
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2009/08/22	A00	28	48	Change U4801 from 72.25X16.A01 to 72.25Q16.001		0909	
		29	48	Del PWR_LED_B AFTE Pad,ADD AFTP5 test point to GND,move EC4802,EC4803			
							0903
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Change List - Power		1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 	

RIYA Discrete Block Diagram

Project code : 91.4CX01.001
PCB P/N : 08267
Revision : -1



CHARGER	
MAX8731AETI-GP 33	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC
SYSTEM DC/DC	
TPS51125RGER-GP 34	
INPUTS	OUTPUTS
+PWR_SRC	+5V_AUX +3.3V_RTC_LDO +5V_ALW +3.3V_ALW
AMD SB700 S5 POWER	
RT9013-12PB-GP 34	
INPUTS	OUTPUTS
+3.3V_ALW	+1.2V_ALW
CPU CORE	
ISL6265AHRTZ-T-GP 35	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE0 +VCC_CORE1 +VDDNB
AMD RS780M CORE	
RT8209BGQW-GP 37	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN
AMD SB700 CORE	
RT8209BGQW-GP 38	
INPUTS	OUTPUTS
+PWR_SRC	+1.2V_RUN
DDR II SUS&VTT	
RT8209BGQW-GP 39	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS
DDR II SUS&VTT	
TPS51100DGQR-GP 39	
INPUTS	OUTPUTS
+1.8V_SUS	+0.9V_VTT
DDR II SUS&VTT	
TPS51100DGQR-GP 41	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE
PCB LAYER	
L1: Top L2: GND L3: Signal L4: Signal L5: VCC L6: Signal L7: GND L8: Bottom	

Main Source

Title

Block Diagram

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Monday, August 24, 2009

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Sheet

2

of

65

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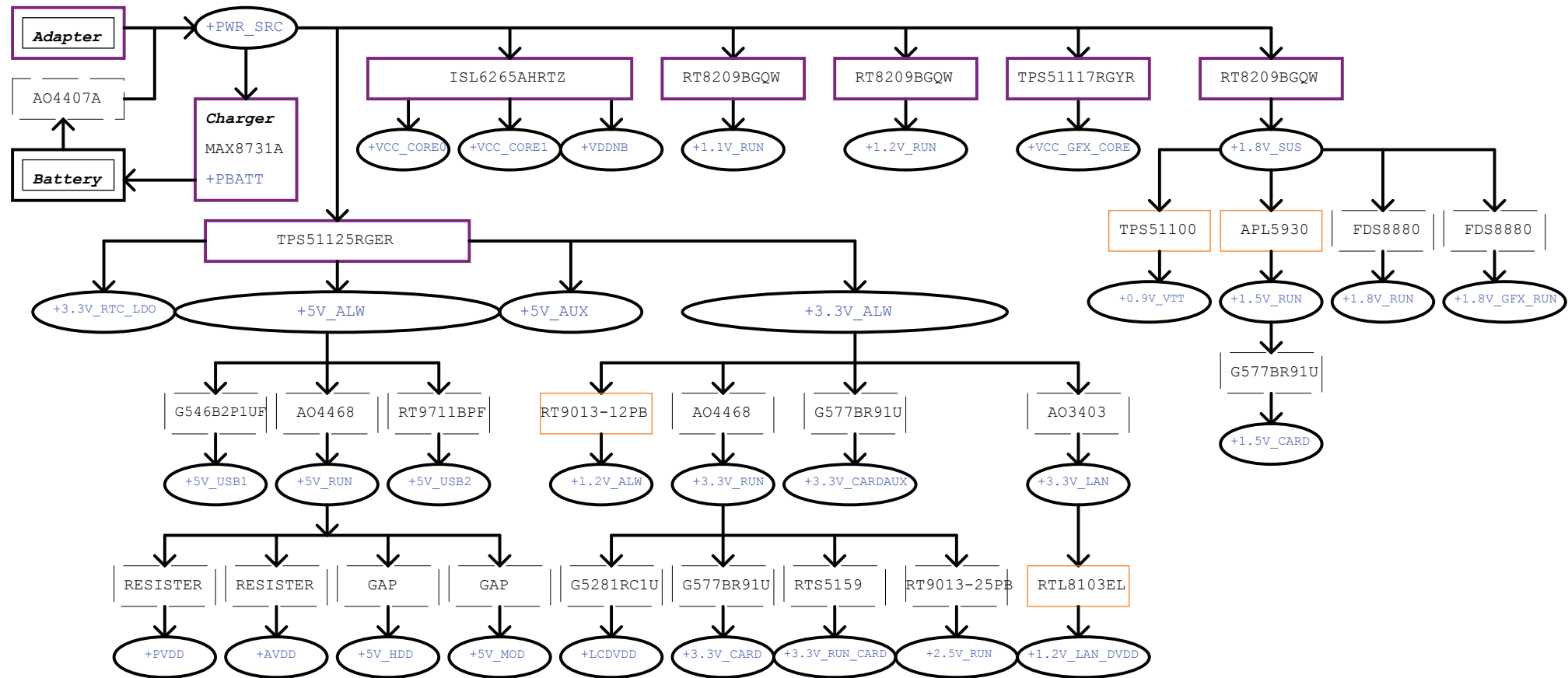
Power Block Diagram

Power Shape

Regulator

LDO

Switch



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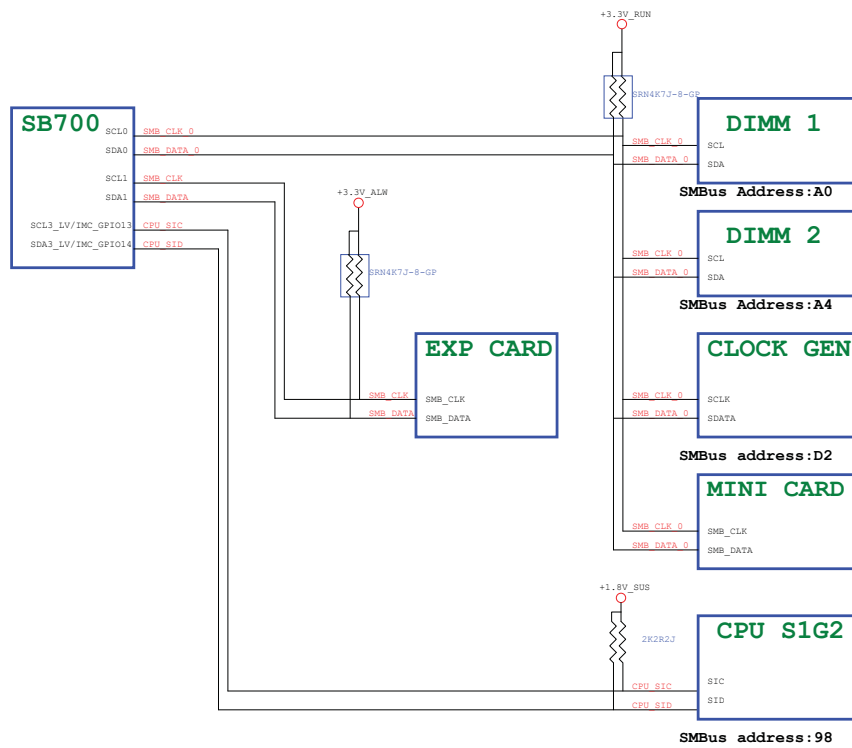
Main Source



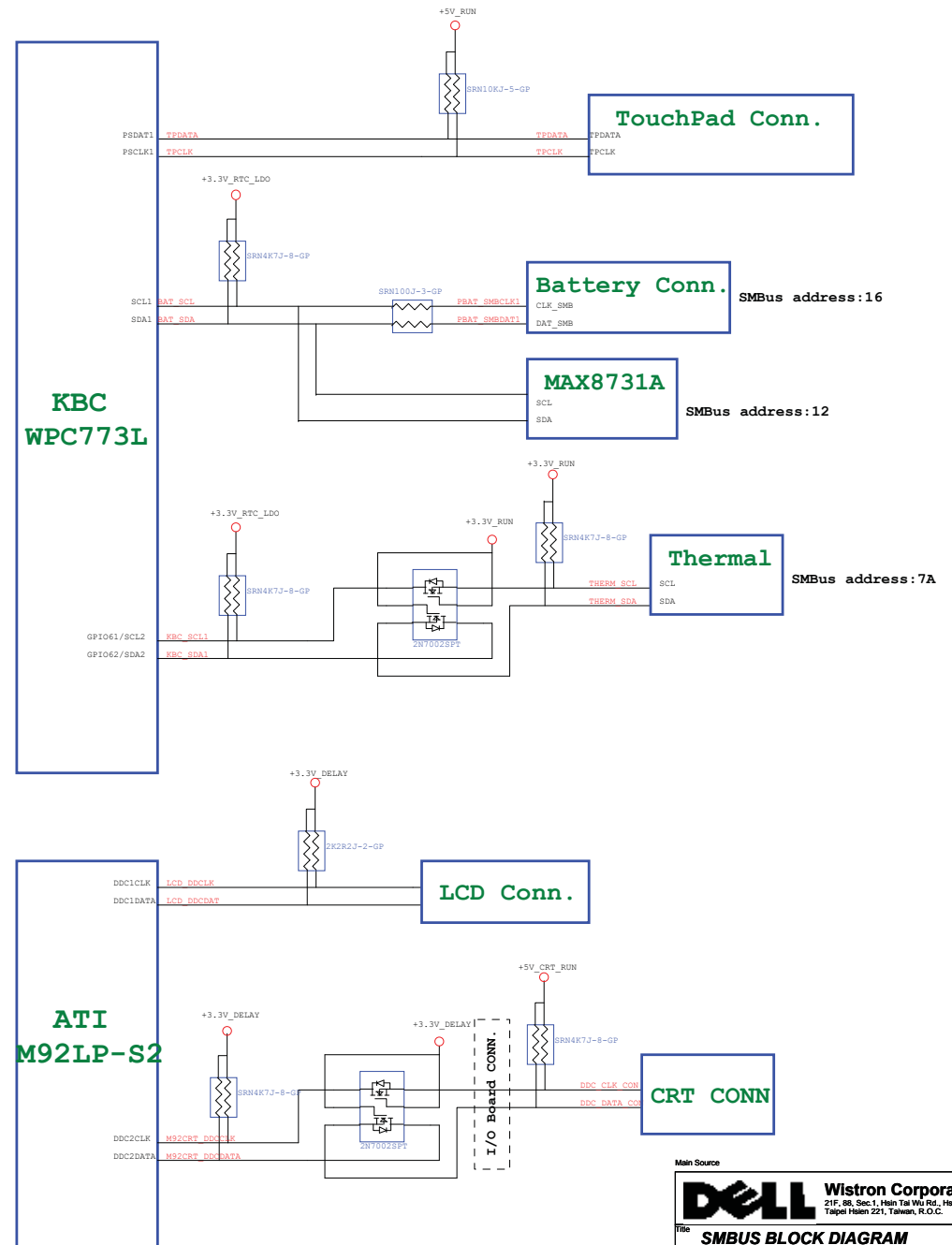
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Title		Power Block Diagram	
Size	Document Number	Rev	
Custom	Riya Discrete	A00	
Date:	Monday, August 24, 2009	Sheet	3 of 65

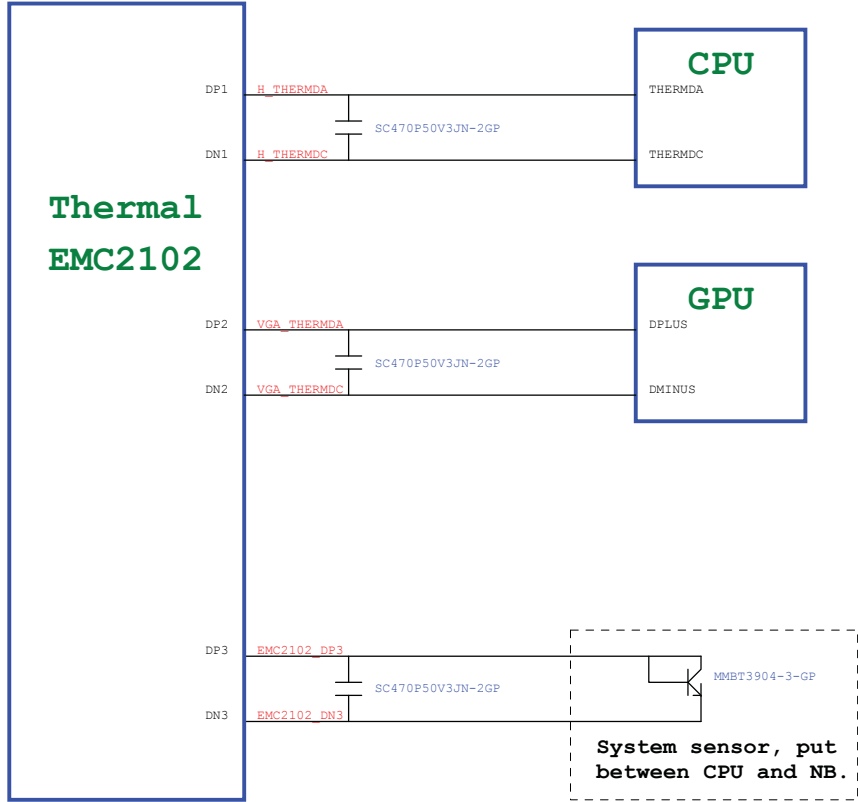
SB700 SMBus Block Diagram



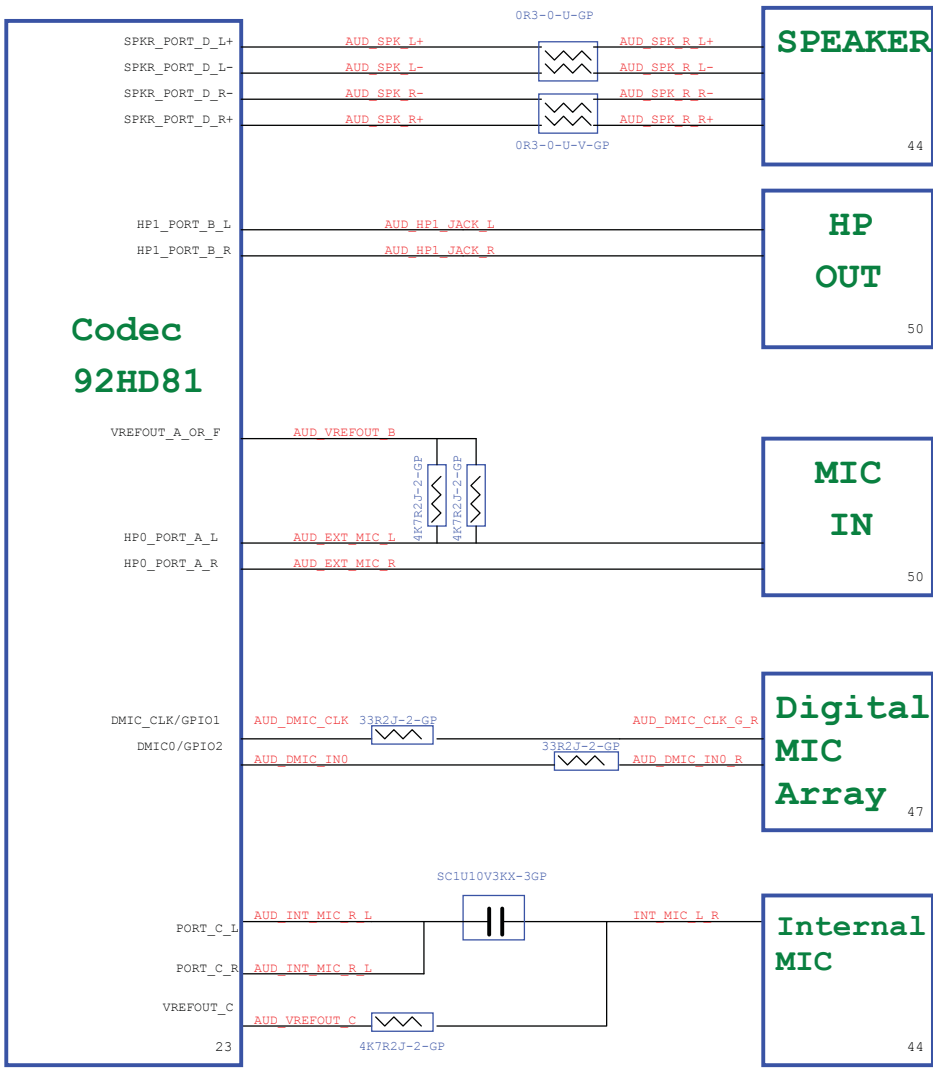
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



SB700 MULTIFUNCTION and GPIO Definitions

SB700 45215_sb710_ds_nda Rev.1.05			
MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
REQ3#/GPIO70	-	I/O	3.3V-5V_S0/15K PU
REQ4#/GPIO71	TP	I/O	3.3V-5V_S0/15K PU
GNT3#/GPIO72	-	I/O	3.3V-5V_S0
GNT4#/GPIO73	TP	I/O	3.3V-5V_S0
INTE#/GPIO33	-	I/O	3.3V-5V_S0/8.2K PU
INTF#/GPIO34	-	I/O	3.3V-5V_S0/8.2K PU
INTG#/GPIO35	-	I/O	3.3V-5V_S0/8.2K PU
INTH#/GPIO36	-	I/O	3.3V-5V_S0/8.2K PU
LDRQ1#/GNT5#/GPIO68	TP	I/O	3.3V-5V_S0/15K PU
BMREQ#/REQ5#/GPIO65	SB700_GPIO65	I/O	3.3V-5V_S0
PCI_PME#/GEVENT4#	TP	I/O	3.3V_S5/10K PU
RI#/EXTENVNT0#	KBC_ECSWI#	I/O	3.3V_S5/10K PU
SLP_S2/GPM9#	TP	I/O	3.3V_S5/10K PD
GA20IN/GEVENT0#	A20GATE	I/O	3.3V-5V_S0/8.2K PU
KBRST#/GEVENT1#	KBRSCIN#	I/O	3.3V-5V_S0/8.2K PU
LPC_PME#/GEVENT3#	KBC_ECSWI#	I/O	3.3V_S5/10K PU
LPC_SMI#/EXTENVNT1#	TP	I/O	3.3V-5V_S0/8.2K PU
S3_STATE/GEVENT5#	-	I/O	3.3V_S5/10K PU
SYS_RESET#/GPM7#	TP	I/O	3.3V_S5/10K PU
WAKE#/GEVENT8#	PCIE_WAKE#	I/O	3.3V_S5/10K PU
BLINK/GPM6#	KBC_ECSMI#	I/O	3.3V_S5/10K PU
SMBALERT#/THRMTrip#/GEVENT2#	SB_THERMTrip#	I/O	3.3V_S5/10K PU
SATA_IS0#/GPIO10	TP	I/O	3.3V-5V_S0
CLK_REQ3#/SATA_IS1#/GPIO6	TP	I/O	3.3V-5V_S0
SMARTVOLT/SATA_IS2#/GPIO4	TP	I/O	3.3V-5V_S0
CLK_REQ0#/SATA_IS3#/GPIO0	TP	I/O	3.3V-5V_S0/10K PD
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39	TP	I/O	3.3V-5V_S0/10K PD
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40	TP	I/O	3.3V-5V_S0/10K PD
SPKR/GPIO2	SB_SPKR	I/O	3.3V-5V_S0
SCL0/GPOC0#	TP	I/O	3.3V-5V_S0
SDA0/GPOC1#	TP	I/O	3.3V-5V_S0
SCL1/GPOC2#	SMB_CLK	I/O	3.3V_S5
SDA1/GPOC3#	SMB_DATA	I/O	3.3V_S5
DDC1_SCL/GPIO9	TP	I/O	3.3V-5V_S0
DDC1_SDA/GPIO8	TP	I/O	3.3V-5V_S0
LLB#/GPIO66	TP	I/O	3.3V_S5/10K PU
SHUTDOWN#/GPIO5	TP	I/O	3.3V-5V_S0
DDR3_RST#/GEVENT7#	-	I/O	3.3V_S5/10K PU
USB_OC6#/IR_TX1/GEVENT6#	TP	I/O	3.3V_S5/10K PU
USB_OC5#/IR_TX0/GPM5#	TP	I/O	OD 3.3V_S5
USB_OC4#/IR_RX0/GPM4#	CPPBE#	I/O	3.3V_S5/10K PU
USB_OC3#/IR_RX1/GPM3#	TP	I/O	3.3V_S5/10K PU
USB_OC2#/GPM2#	TP	I/O	3.3V_S5/10K PU
USB_OC1#/GPM1#	USB_OC_2_#	I/O	3.3V_S5/10K PU
USB_OC0#/GPM0#	USB_OC_01_#	I/O	3.3V_S5/10K PU
SCL0/GPOC0#	TP	I/O	3.3V-5V_S0
SDA0/GPOC1#	TP	I/O	3.3V-5V_S0
SCL1/GPOC2#	SMB_CLK	I/O	3.3V_S5
SDA1/GPOC3#	SMB_DATA	I/O	3.3V_S5
AZ_SDIN0/GPIO42	SB_AZ_CODECS_SDIN0	I/O	3.3V_S5/50K PD
AZ_SDIN1/GPIO43	-	I/O	3.3V_S5/50K PD
AZ_SDIN2/GPIO44	-	I/O	3.3V_S5/50K PD
AZ_SDIN3/GPIO46	-	I/O	3.3V_S5/50K PD
AZ_DOCK_RST#/GPM8#	-	I/O	10K PU
SPI_CS2#/IMC_GPIO2	TP	I/O	3.3V_S5/10K PU
IDE_RST#/F_RST#/IMC_GPIO3	IDE_RST#	OD	3.3V-5V_S5
IMC_GPIO4	TP	I/O	3.3V-5V_S5
IMC_GPIO5	TP	I/O	3.3V-5V_S5
IMC_GPIO6	TP	I/O	3.3V-5V_S5
IMC_GPIO7	TP	I/O	3.3V-5V_S5
IMC_GPIO8	-	I/O	3.3V_S5
IMC_GPIO9	-	I/O	3.3V_S5
IMC_PWM0/IMC_GPIO10	-	I/O	3.3V_S5
SCL2/IMC_GPIO11	-	OD	3.3V-5V_S5
SDA2/IMC_GPIO12	-	OD	3.3V-5V_S5
SCL3_LV/IMC_GPIO13	CPU_SIC	OD	3.3V_S5
SDA3_LV/IMC_GPIO14	CPU_SID	OD	3.3V_S5
IMC_PWM1/IMC_GPIO15	-	I/O	3.3V_S5
IMC_PWM2/IMC_GPIO16	SB_GPO16	I/O	3.3V-5V_S5
IMC_PWM3/IMC_GPIO17	SB_GPO17	I/O	3.3V-5V_S5
IMC_GPIO18	-	I/O	3.3V_S5
IMC_GPIO19	-	I/O	3.3V_S5
IMC_GPIO20	-	I/O	3.3V_S5
IMC_GPIO21	-	I/O	3.3V_S5

SB700 45215_sb710_ds_nda Rev.1.05			
MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
IMC_GPIO22	-	I/O	3.3V_S5
IMC_GPIO23	-	I/O	3.3V_S5
IMC_GPIO24	-	I/O	3.3V_S5
IMC_GPIO25	-	I/O	3.3V_S5
IMC_GPIO26	-	I/O	3.3V_S5
IMC_GPIO27	-	I/O	3.3V_S5
IMC_GPIO28	-	I/O	3.3V_S5
IMC_GPIO29	-	I/O	3.3V_S5
IMC_GPIO30	-	I/O	3.3V_S5
IMC_GPIO31	-	I/O	3.3V_S5
IMC_GPIO32	-	I/O	3.3V_S5
IMC_GPIO33	-	I/O	3.3V_S5
IMC_GPIO34	-	I/O	3.3V_S5
IMC_GPIO35	-	I/O	3.3V_S5
IMC_GPIO36	-	I/O	3.3V_S5
IMC_GPIO37	-	I/O	3.3V_S5
IMC_GPIO38	-	I/O	3.3V_S5
IMC_GPIO39	-	I/O	3.3V_S5
IMC_GPIO40	-	I/O	3.3V_S5
IMC_GPIO41	-	I/O	3.3V_S5
SATA_ACT#/GPIO67	TP	I/O	
IDE_D0/GPIO15	-	I/O	
IDE_D1/GPIO16	-	I/O	
IDE_D2/GPIO17	-	I/O	
IDE_D3/GPIO18	-	I/O	
IDE_D4/GPIO19	-	I/O	
IDE_D5/GPIO20	-	I/O	
IDE_D6/GPIO21	-	I/O	
IDE_D7/GPIO22	-	I/O	
IDE_D8/GPIO23	-	I/O	
IDE_D9/GPIO24	-	I/O	
IDE_D10/GPIO25	-	I/O	
IDE_D11/GPIO26	-	I/O	
IDE_D12/GPIO27	-	I/O	
IDE_D13/GPIO28	-	I/O	
IDE_D14/GPIO29	-	I/O	
IDE_D15/GPIO30	-	I/O	
SPI_DI/GPIO12	TP	I/O	3.3V_S5/10K PD
SPI_DO/GPIO11	TP	I/O	3.3V_S5/10K PD
SPI_CLK/GPIO47	TP	I/O	3.3V_S5/10K PD
SPI_HOLD#/GPIO31	TP	I/O	3.3V_S5/10K PU
SPI_CS#/GPIO32	TP	I/O	3.3V_S5/10K PU
LAN_RST#/GPIO13	TP	I/O	3.3V-5V_S0
ROM_RST#/GPIO14	TP	I/O	3.3V-5V_S0
FANOUT0/GPIO3	TP	I/O	3.3V-5V_S0/8.2K PU
FANOUT1/GPIO48	SB_GPIO48	I/O	3.3V-5V_S0/8.2K PU
FANOUT2/GPIO49	TP	I/O	3.3V-5V_S0/8.2K PU
FANIN0/GPIO50	-	I/O	3.3V-5V_S0
FANIN1/GPIO51	TP	I/O	3.3V-5V_S0
FANIN2/GPIO52	TP	I/O	3.3V-5V_S0
TEMPIN0/GPIO61	TP	I/O	3.3V_S5
TEMPIN1/GPIO62	-	I/O	3.3V_S5
TEMPIN2/GPIO63	-	I/O	3.3V_S5
TEMPIN3/TALERT#/GPIO64	TALERT#	I/O	3.3V_S5
VIN0/GPIO53	-	I/O	3.3V_S5
VIN1/GPIO54	-	I/O	3.3V_S5
VIN2/GPIO55	-	I/O	3.3V_S5
VIN3/GPIO56	-	I/O	3.3V_S5
VIN4/GPIO57	-	I/O	3.3V_S5
VIN5/GPIO58	-	I/O	3.3V_S5
VIN6/GPIO59	-	I/O	3.3V_S5
VIN7/GPIO60	-	I/O	3.3V_S5

WPCE773L MULTIFUNCTION and GPIO Definitions

WPCE773L Preliminary Datasheet - Revision 0.8			
MULTIFUNCTION PINS	FUNCTION	I/O	POWER DOMAIN
GPIO101/TB2	PM_SLP_S3#	I/O	3.3V-5V_AUX
GPIO03	KBC_PWRBTN#	I/O	3.3V_AUX
GPIO04	SYS_THERMTrip#	I/O	3.3V_AUX
GPIO05	LCD_EC_DET	I/O	3.3V_AUX
GPIO06	AC_IN#	I/O	3.3V-5V_AUX
GPIO07	LID_CLOSE#	I/O	3.3V_AUX
GPIO10/LPCPD#	ADAPT_TRIP_SEL	I/O	3.3V-5V_AUX
GPIO11/CLKRUN#	PM_CLKRUN#	I/O	3.3V-5V_AUX
GPIO12/PSDAT3	KB_DET#	I/O	3.3V-5V_AUX
GPIO13/C_PWM	BRIGHTNESS	I/O	3.3V-5V_AUX
GPIO14/TB1	PSID_EC	I/O	3.3V-5V_AUX
GPIO15/A_PWM	KBC_BEEP	I/O	3.3V-5V_AUX
GPIO16	PM_LAN_ENABLE	I/O	3.3V-5V_AUX
GPIO17/SCL1	BAT_SCL	I/O	3.3V-5V_AUX
GPIO20/TA2	PM_PWRBTN#	I/O	3.3V-5V_AUX
GPIO21/B_PWM	BATLOW_LED	I/O	3.3V-5V_AUX
GPIO22/SDA1	BAT_SDA	I/O	3.3V-5V_AUX
GPIO23	1.8V_GFX_RUN_PWRGD#	I/O	3.3V-5V_AUX
GPIO25/PSCLK3	LCD_CBL_DET#	I/O	3.3V-5V_AUX
GPIO26/PSCLK2	LCD_TST	I/O	3.3V-5V_AUX
GPIO30	EC_SPI_WP#_R	I/O	3.3V-5V_AUX
GPIO31	RUNPWROK	I/O	3.3V-5V_AUX
GPIO32/D_PWM	PWRLED	I/O	3.3V-5V_AUX
GPIO33/H_PWM	HP_MUTE	I/O	3.3V-5V_AUX
GPIO35/PSDAT1	TPDATA	I/O	3.3V-5V_AUX
GPIO36	S5_ENABLE	I/O	3.3V-5V_AUX
GPIO37/PSCLK1	TPCLK	I/O	3.3V-5V_AUX
GPIO40/F_PWM	3.3V_DELAY_EN	I/O	3.3V-5V_AUX
GPIO41	BAT_IN#	I/O	3.3V-5V_AUX
GPIO42/TCK	AD_OFF	I/O	3.3V-5V_AUX
GPIO43/TMS	KBC_RSMRST#	I/O	3.3V-5V_AUX
GPIO44/TDI	PM_SLP_S5#	I/O	3.3V-5V_AUX
GPIO45/E_PWM	KBC_PLTRST_DELAY#	I/O	3.3V-5V_AUX
GPIO46/TRST#	3V_5V_POK	I/O	3.3V-5V_AUX
GPIO50/TDO	PSID_DISABLE#	I/O	3.3V-5V_AUX
GPIO52/RDY#	BLON_OUT	I/O	3.3V-5V_AUX
ECSCI#/GPIO54	KBC_D_ECSCI#	I/O	3.3V-5V_AUX
GPIO55/CLKOUT	AMP_MUTE#	I/O	3.3V_AUX
GPIO56/TA1	LCD_TST_EN	I/O	3.3V-5V_AUX
GPIO65/SMI#	PANEL_BKEN	I/O	3.3V-5V_AUX
GPIO66/G_PWM	1.8V_GFX_RUN_EN	I/O	3.3V-5V_AUX
GPIO67/PWREQ#	KBC_D_ECSWI#	I/O	3.3V-5V_AUX
GPIO70	KBC_D_ECSMI#	I/O	3.3V-5V_AUX
GPIO71	GFX_CORE_EN	I/O	3.3V-5V_AUX
GPIO73/SCL2	KBC_SCL1	I/O	3.3V-5V_AUX
GPIO74/SDA2	KBC_SDA1	I/O	3.3V-5V_AUX
GPIO75	WIFI_RF_EN	I/O	3.3V-5V_AUX
GPIO76/SHBM	KBC_SHBM	O	3.3V-5V_AUX
GPIO77	BLUETOOTH_EN	I/O	3.3V-5V_AUX
GPIO81	1.1V_GFX_RUN_EN	I/O	3.3V-5V_AUX
GPO82/TRIS#	USB_PWR_EN#	O	3.3V-5V_AUX
GPO83/SOUT_CR/BADDR1	E51_TxD	O	3.3V-5V_AUX
GPIO87/SIN_CR	E51_RxD	I/O	3.3V-5V_AUX
GPIO90/AD0	AD_IA	I	3.3V_AUX
GPIO92/AD2	THERMTrip_VGA#	I	3.3V_AUX
GPIO93/AD3	ADAPT_OC	I	3.3V_AUX
GPIO94	PCB_VER0	I	3.3V_AUX
GPIO95	PCB_VER1	I	3.3V_AUX
GPIO96	PCB_VER2	I	3.3V_AUX
GPIO97	CAMERA_DET#	I	3.3V_AUX

USB Table

Pair	Controllers	Device
0	EHCI Dev.19	I/O BOARD Left Side
1		I/O BOARD Left Side
2		Camera
3		RESERVED
4		Express Card
5	EHCI Dev.18	RESERVED
6		BLUETOOTH
7		RESERVED
8		RESERVED
9		Card Reader
10	EHCI Dev.17	MINI CARD
11		USB Port Right Side
12	OHCI Dev.20	RESERVED
13		RESERVED

PCIE Routing

Pair	Device
PE_GPP1	LAN
PE_GPP2	MINI Card
PE_GPP3	EXP Card

CIRCUIT NOTE

For Circuit
For Layout
For EMI

Table of Content

Size A2

Monday, August 24, 2009

Document Number

Rev A00

Wistron Corporation

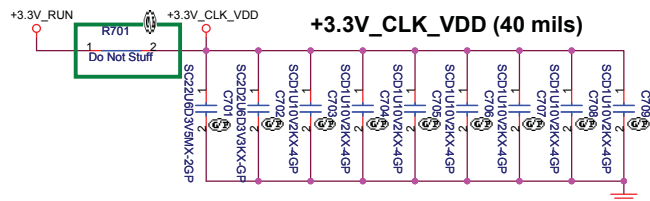
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.

Table of Content

Rev A00

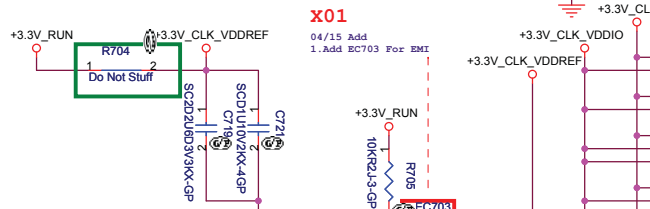
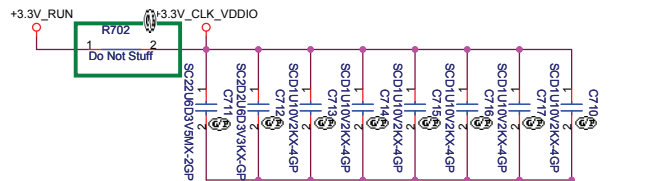
SSID = CLOCK

1'nd 68.00084.A31 (MURATA)
2'nd

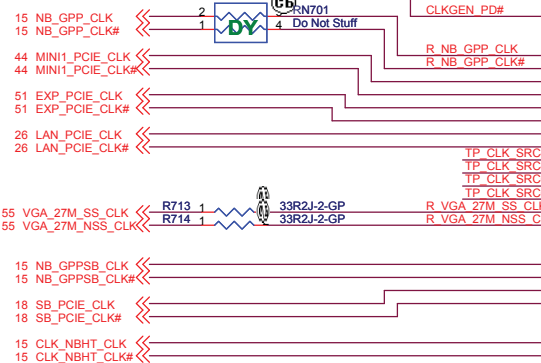


A00

8/24
Change R701,R702,R704 from 0 ohm to short pad



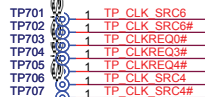
NBGP (100MHz)
WLAN (100MHz)
EXP (100MHz)
LAN (100MHz)
VGA (27MHz)



71.08628.003

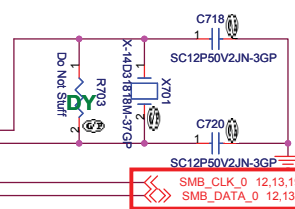
A00

08/22 modify
change U702 to 71.08628.003.
2nd source is 71.09480.A03



XTAL

1'nd 82.30005.901
2'nd 82.30005.A51



CLKREQ# MAP

CLKREQ0#	No use
CLKREQ1#	CLKSRC1 MINI1
CLKREQ2#	CLKSRC2 EXPCARD
CLKREQ3#	No use
CLKREQ4#	No use

X01

04/08 modify
1.Change Clk gen,Mini Card SMBus from Ch1 to Ch0

VGA (100MHz)

CPU_CLK (200MHz)

CardReader (48MHz)
SB700_USB (48MHz)

NB OSCIN (14MHz)

SB OSCIN (14MHz)

OSC_14M_NB	
RS780M	1.1V 158R/90.9R

SB TYPE	R716
*SB700	EMPTY
SB710	STUFF

*DEFAULT

X01

03/31 modify
1.Change R709/R710 from 33 ohm to 22 ohm

NB ALINK
(100MHz)
SB PCIE
(100MHz)
VGA M92
(27MHz)

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27MHz FS2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock

Main Source

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
Clock Generator ICS9LPRS480			A00
Size	Document Number		
Custom	Riya Discrete		
Date:	Tuesday, August 25, 2009	Sheet	7 of 65

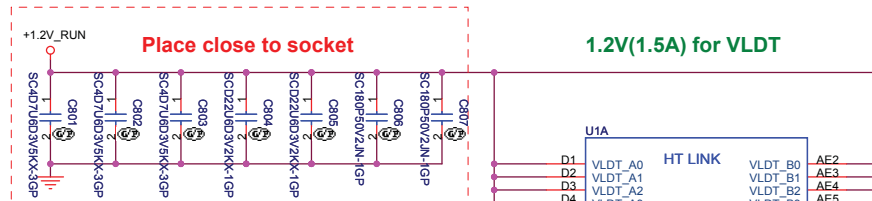
www.vinafix.vn

SSID = CPU

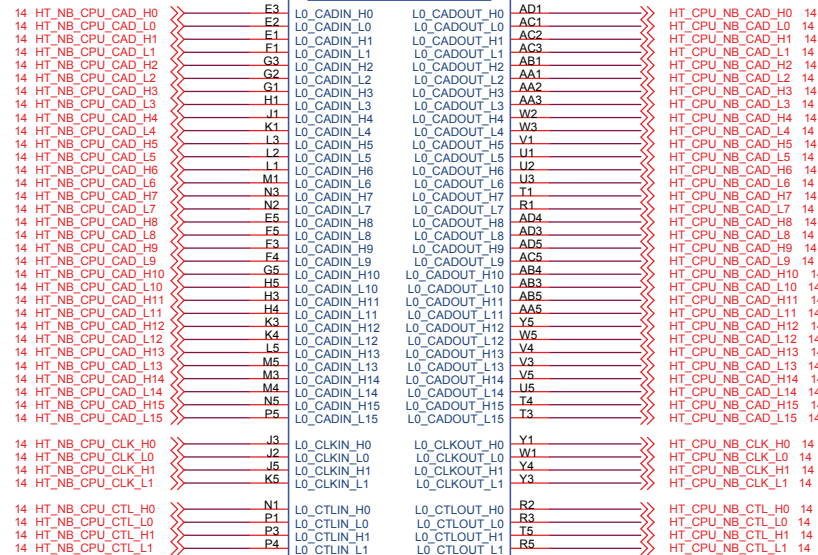
CPU TYPE	C801~C803
*Griffin	4.7uF
Tigris	10uF

*DEFAULT

CPU HT3.0



State	Specification	Notes	2M200100M2303
S0.C0.P.x	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD



SKT-CPU638P-GP-U2
62.10055.111

SKT-BGA638H176

1'nd 62.10055.111

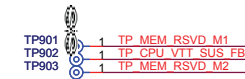
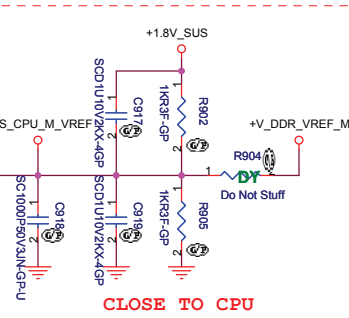
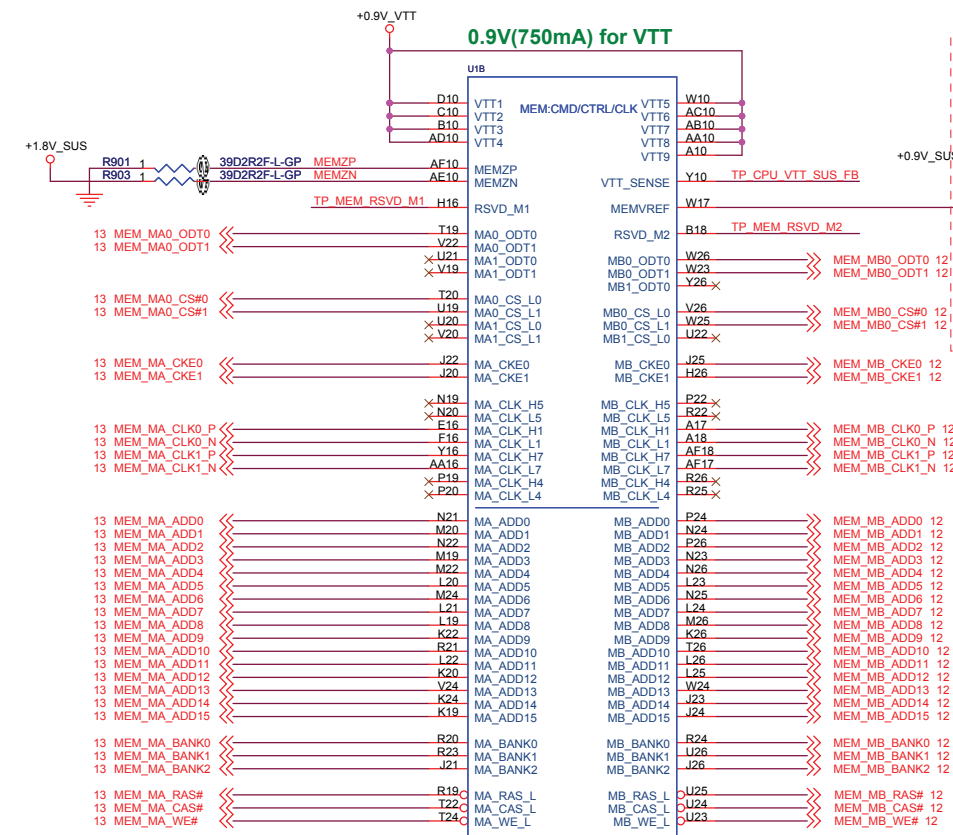
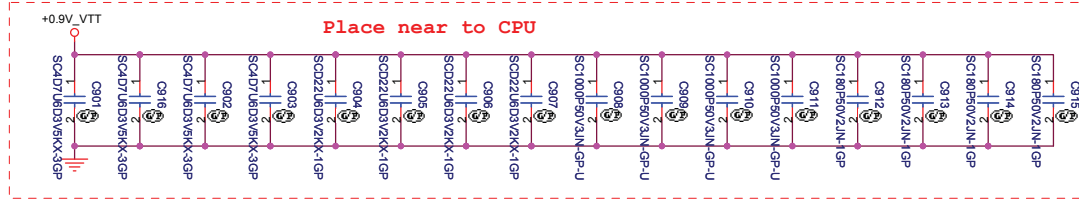
2'nd 62.10055.171

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Main Source

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CPU HT_LINK I/F_(1/4)			
Size	Document Number	Rev	
Custom	Riya Discrete		A00
Date:	Wednesday, August 26, 2009	Sheet	8 of 65

SSID = CPU



SKT-CPU638P-GP-U2
62.10055.111

SKT-CPU638P-GP-U2
62.10055.111

Main Source



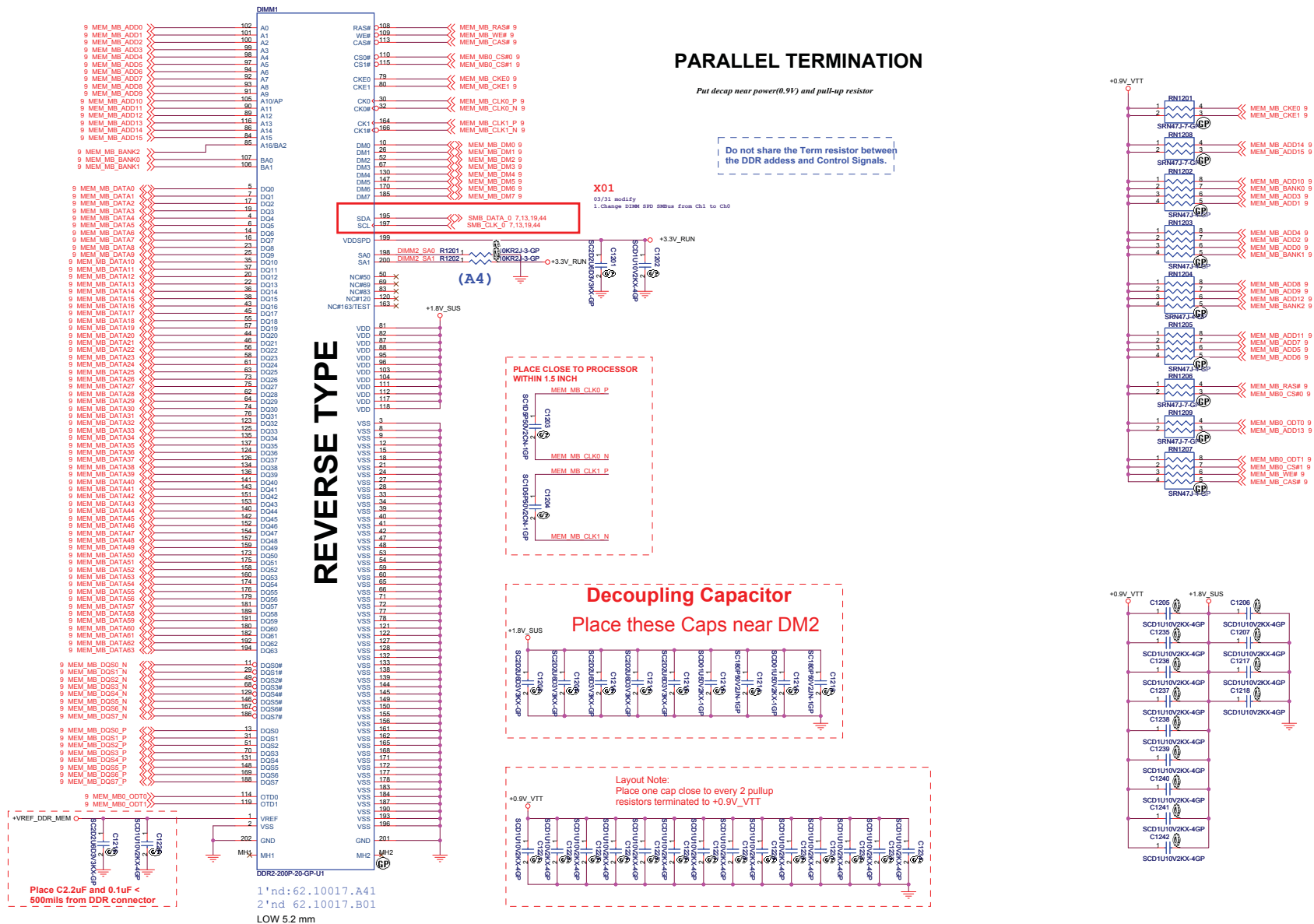
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File CPU_DDR_(2/4)

Size Document Number Rev
Custm Riya Discrete A00

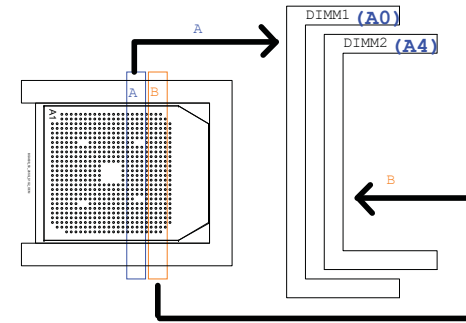
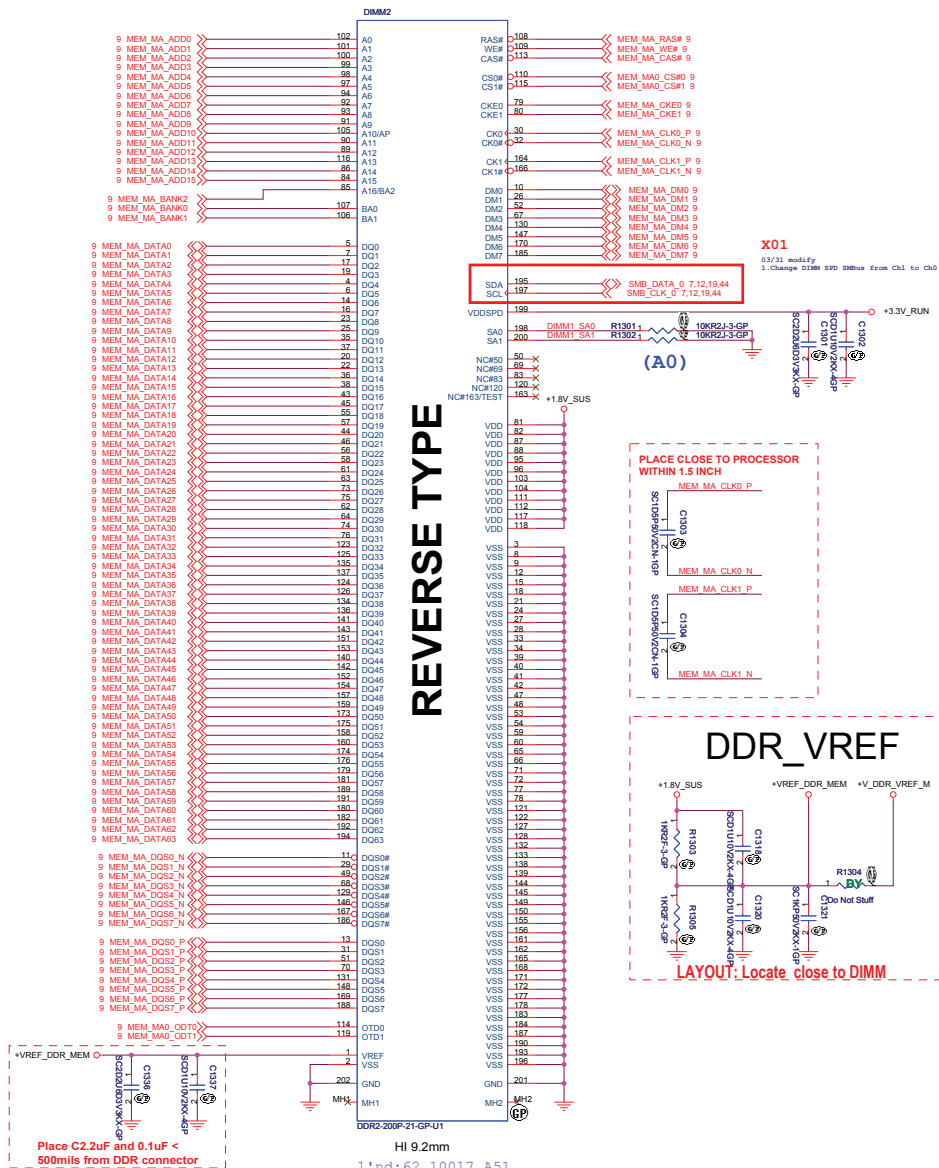
Date: Wednesday, August 26, 2009 Sheet 9 of 65

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Main Source

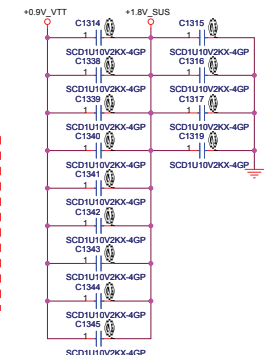
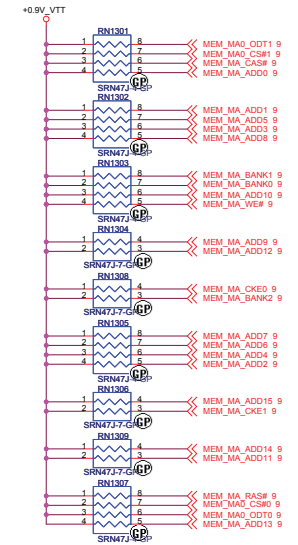
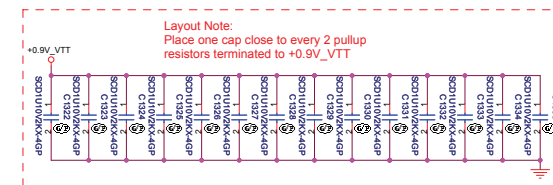
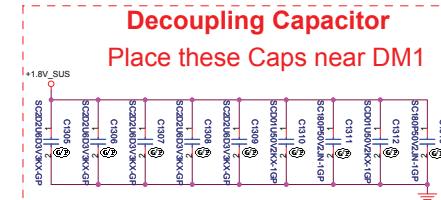
SSID = MEMORY



PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR address and Control Signals.



Main Source

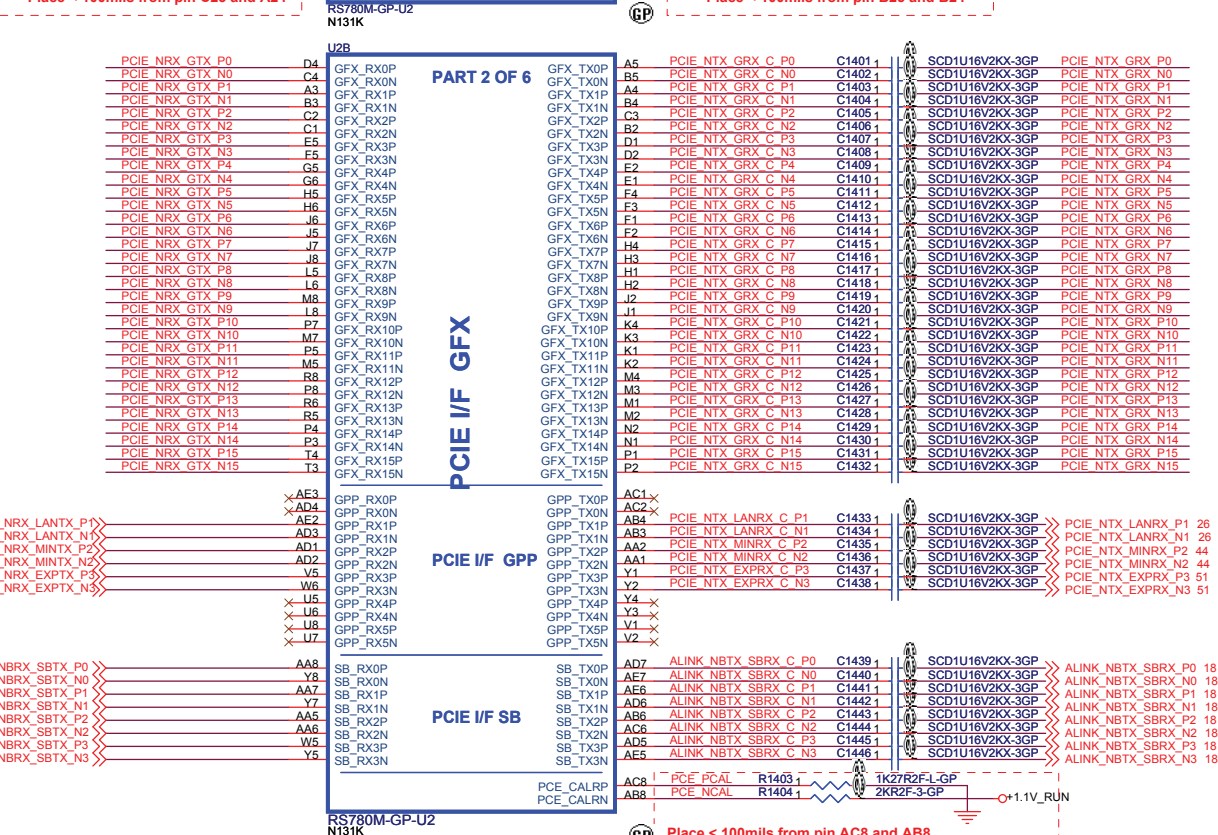
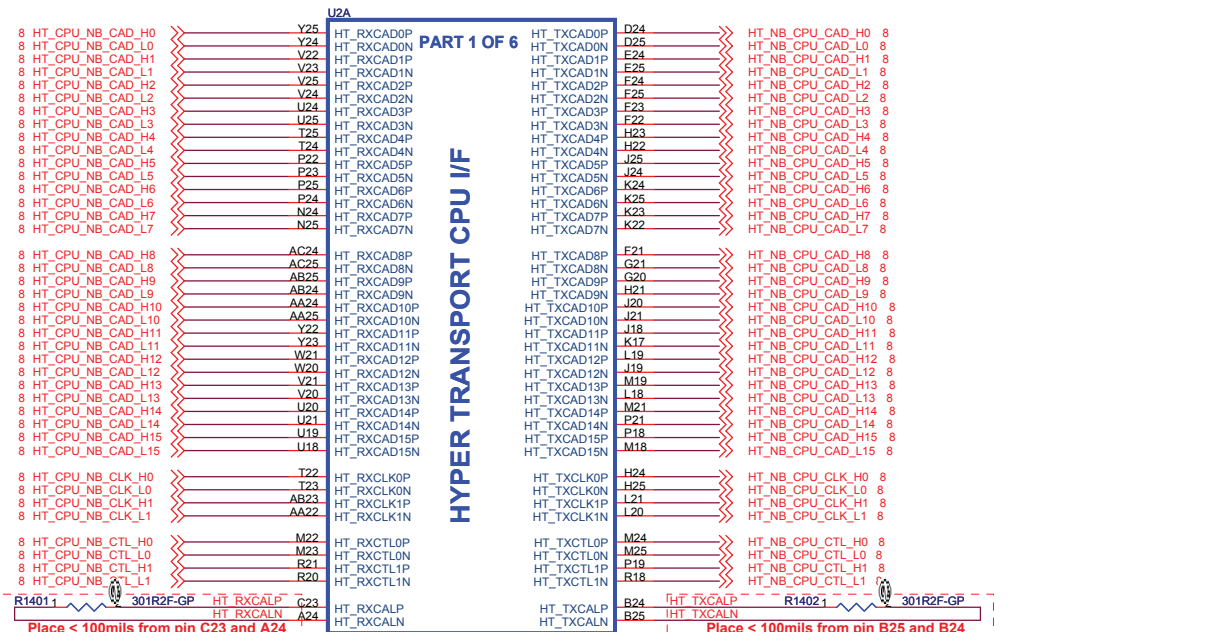
DELL Wistron Corporation
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

File: **DDR DIMM2**
Size: **A2** Document Number: **Riya Discrete** Rev: **A00**
Date: **Wednesday, August 26, 2009** Sheet: **13** of **85**

www.vinafix.vn

SSID = N.B

RS780M A13 : 71.RS780.M11



LAN
WLAN
EXP

A-LINK

LAN
WLAN
EXP

A-LINK

Main Source

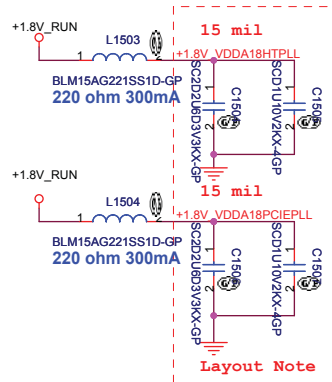
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS780M_HT LINK&PCIe(1/4)**

Size: Document Number
Custpm: **Riya Discrete**

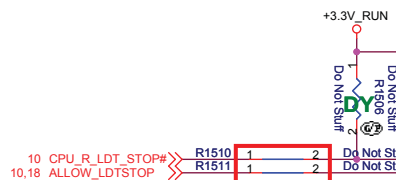
Date: Thursday, September 03, 2009 Sheet 14 of 65

SSID = N.B



A00
8/22
Change R1509 from 0 ohm to short pad

X01
04/17 Del
1. Del R1508, No reserve



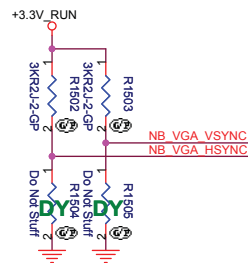
X01
04/14 Del
1. Del R1510
Del R1511
reserve closed-gap.
reserve closed-gap.

GPIO MODE

STRP_DATA	VCC_NB
* 1	1.0V
0	1.1V

*DEFAULT

TP1501 1 TP NB DDC DATA0
TP1502 1 TP NB DDC CLK0
TP1503 1 TP NB DDC CLK1
TP1504 1 TP NB DDC DATA1
TP1505 1 TP NB RESERVED



STRAP_DEBUG_BUS_GPIO_ENABLE# (RS780M use DAC_VSYNC)

Enables debug bus access through memory I/O pads and GPIOs.
0 : Enable * 1 : Disable

SIDE_PORT_EN# (RS780M use DAC_HSYNC)

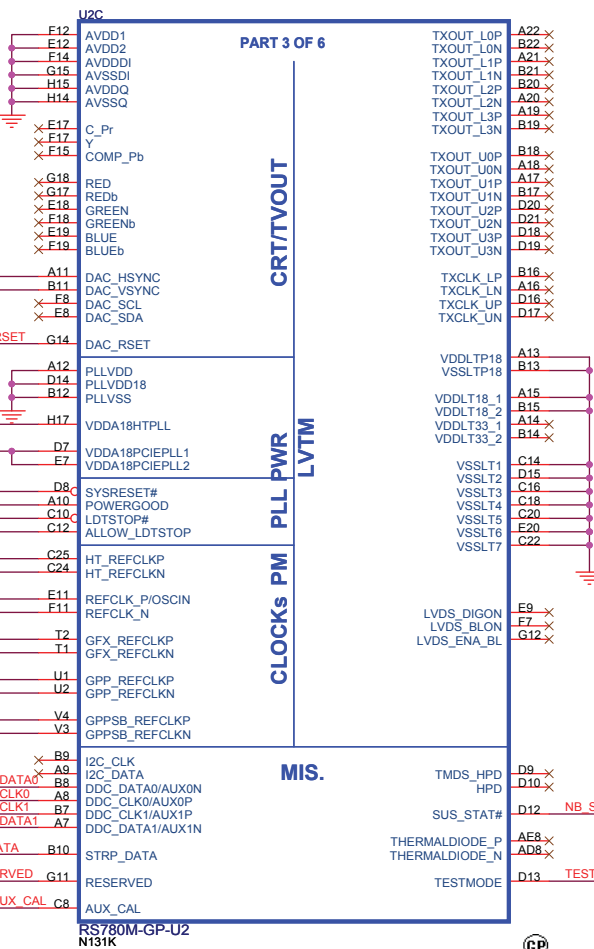
0 : Available * 1 : Not available

LOAD_EEPROM_STRAPS# (RS780M use SUS_STAT#)

Selects Loading of STRAPS From EEPROM

* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

*DEFAULT



Main Source

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

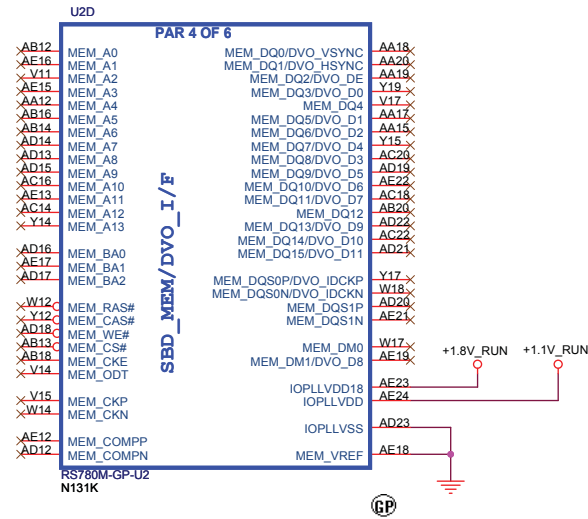
Title **ATI-RS780M_LVDS&CRT_(2/4)**

Size A3 Document Number **Riya Discrete** Rev **A00**

Date: Thursday, September 03, 2009 Sheet 15 of 65

www.vinafix.vn

SSID = N.B



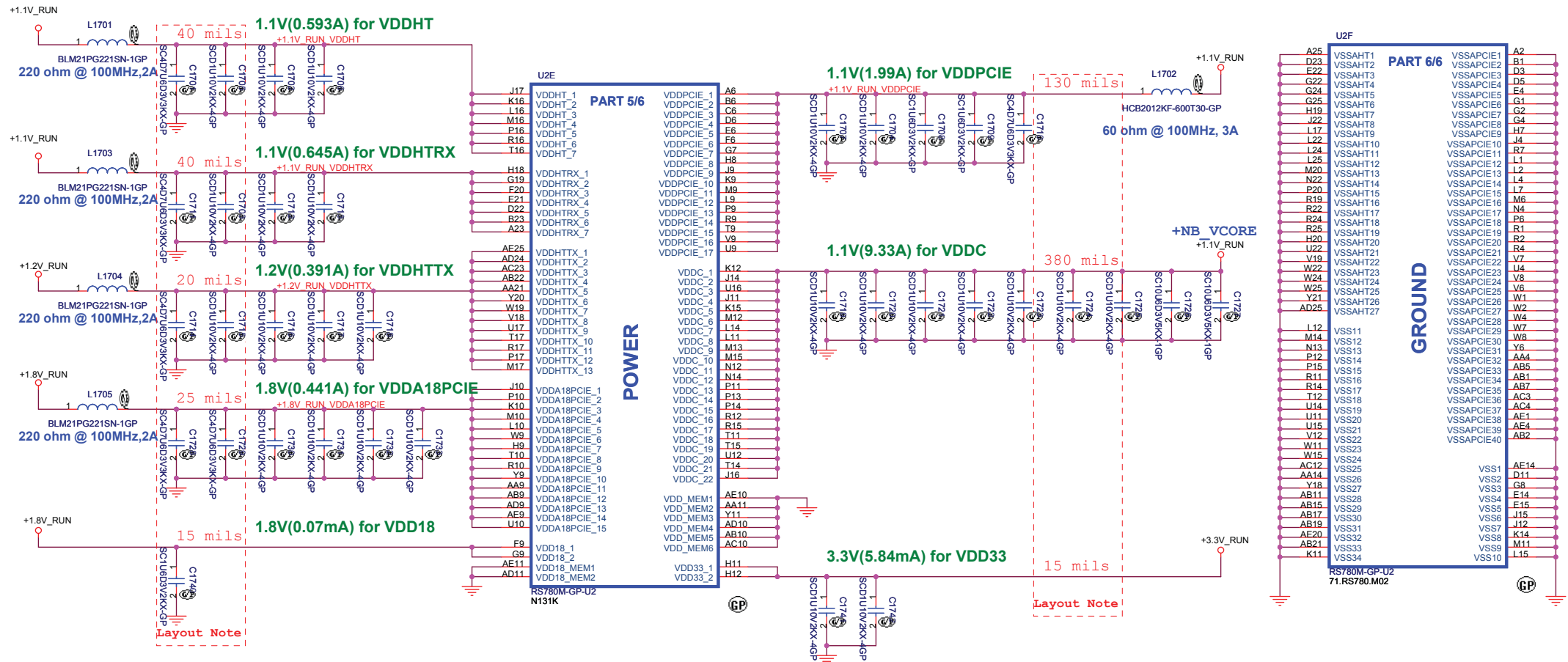
Main Source



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ATi-RS780M_SidePort_(3/4)		
Size A3	Document Number Riya Discrete	Rev A00
Date: Thursday, September 03, 2009	Sheet 16 of 65	

SSID = N.B



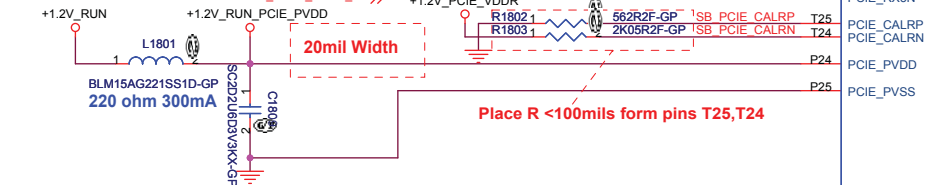
Main Source



ATi-RS780M_PWR&GD_(4/4)

Size A3 Document Number Riya Discrete Rev A00 Date Thursday, September 03, 2009 Sheet 17 of 65

SB700 A12 : 71.SB700.M05

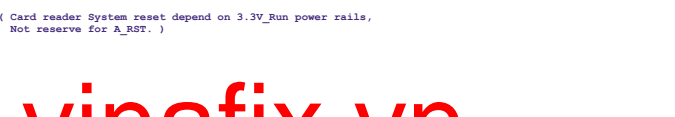
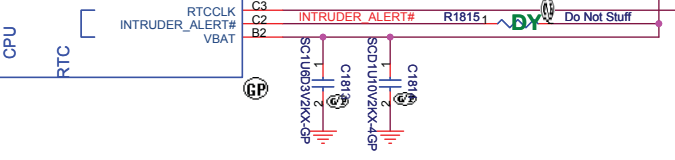
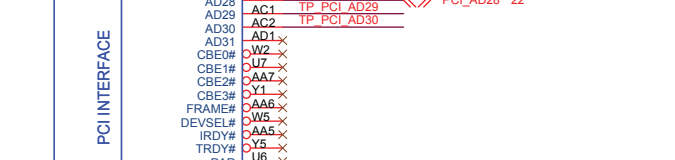
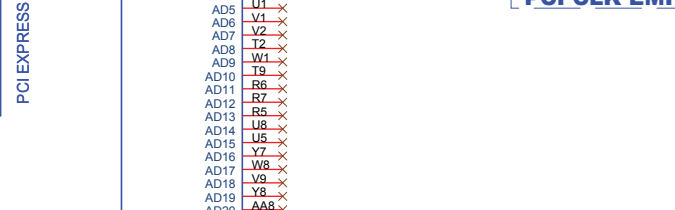
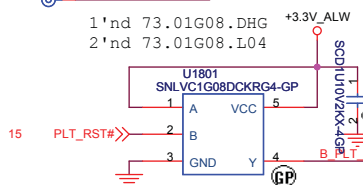


Place R <100mils from pins T25,T24



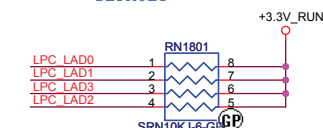
CPU TYPE	R1813
*Griffin	300 ohm
Tigris	1K ohm

*DEFAULT



SB TYPE	RN1801
*SB700	STUFF
SB710	EMPTY

*DEFAULT



LPC Bus Routing first connects to MINICARD then connects to KBC

LPC_LAD0 27,44
LPC_LAD1 27,44
LPC_LAD2 27,44
LPC_LAD3 27,44
LPC_LFRAME# 27,44



Main Source



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

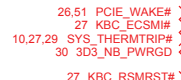
Title	ATi-SB700 PCIE&PCI (1/5)
-------	-------------------------------------

Size	Document Number	Rev
------	-----------------	-----

A3	<i>Riya Discrete</i>	A
----	-----------------------------	---

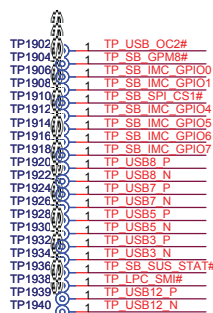
www.vinafix.vn

SSID = S.B



```
03/31 modify
1.Change DIMM SPD SMBus from Ch1 to Ch0
04/08 modify
1.Change Clk gen,Mini Card SMBus from Ch1 to Ch0
```

8/22
Change R1907, R1920,R1921 from 0 ohm to short pad



DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

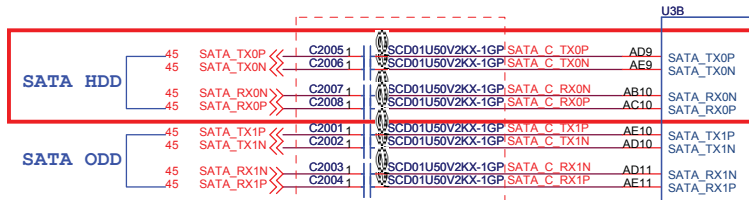
Title			
ATi-SB700_USB&GPIO_(2/5)			
Size	Document Number	Rev	
Custom	Riya Discrete	A0	
Date:	Thursday, September 03, 2009	Sheet 19 of	65

www.vinafix.vn

SSID = S.B

X01

04/06 modify
1. Change SATA HD from Port-3 to Port-0



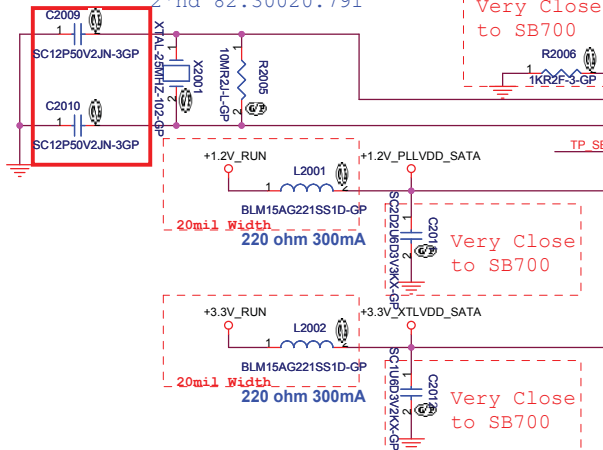
PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

X01

04/06 modify
1. Change C2009/C2010 from 10P to 12P

XTAL

1'nd 82.30020.851
2'nd 82.30020.791



Very Close,
to SB700

Very Close
to SB700

Very Close
to SB700

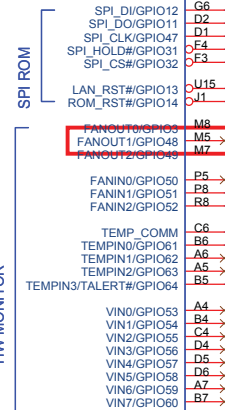
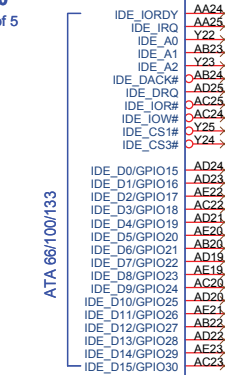
SB700
Part 2 of 5

SERIAL ATA

SATA PWR

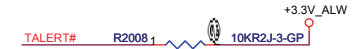
HW MONITOR

SB700-1-GP-U1
Y708D



X01

04/02 modify
1. Add SB GPIO48 To detect LCD Size
06/09 modify
1. Del R2009 R2010



A00

8/24
Change L2003 from 0 ohm to short pad

Layout Notice connect
to cap then Gnd

TP2001	1	TP ROM RST#
TP2002	1	TP SPI DI
TP2003	1	TP SPI DO
TP2004	1	TP SPI CLK
TP2005	1	TP SPI HOLD#
TP2006	1	TP SPI CS#
TP2007	1	TP SB SATA ACT#
TP2008	1	TP SB GPIO13
TP2009	1	TP SB GPIO3
TP2011	1	TP SB GPIO49
TP2012	1	TP SB GPIO50
TP2013	1	TP SB GPIO52
TP2014	1	TP SB GPIO61

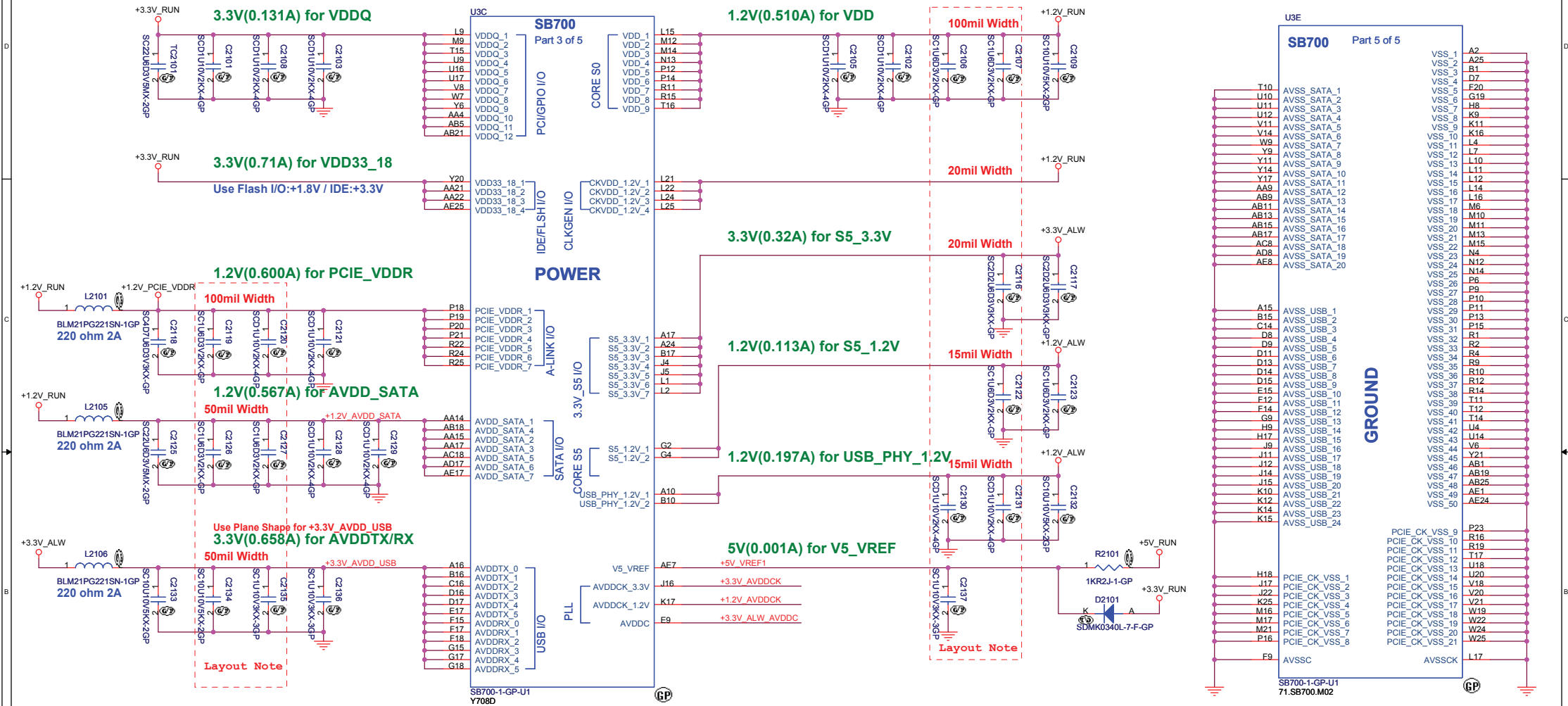
www.vinafix.vn

Main Source



Title ATi-SB700_SATA-IDE_(3/5)		
Size Custom	Document Number Riya Discrete	Rev A00
Date: Thursday, September 03, 2009	Sheet 20 of 65	

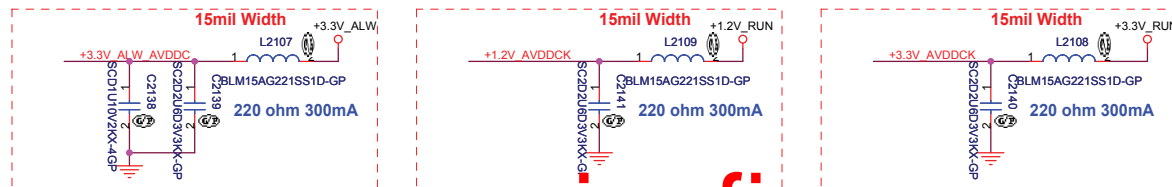
SSID = S.B



3.3V(0.017A) for AVDDC

1.2V(0.062A) for AVDDCK_1.2V

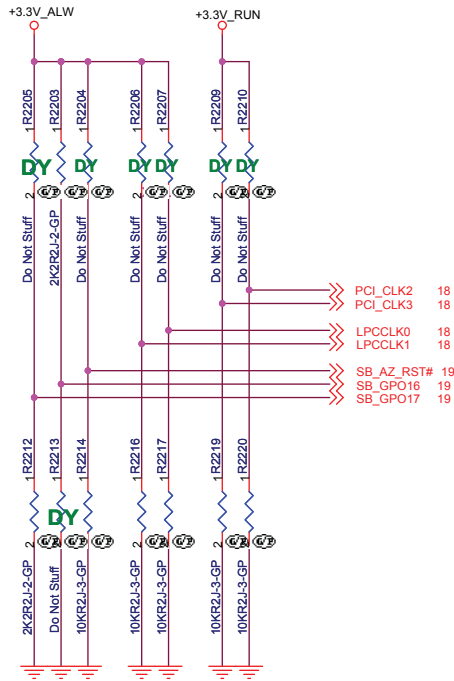
3.3V(0.047A) for AVDDCK_3.3V



Main Source

SSID = S.B

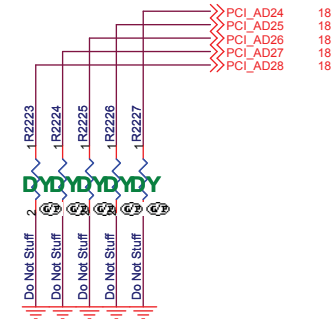
REQUIRED STRAPS



REQUIRED SYSTEM STRAPS

	PCI_CLK2	PCI_CLK3	LPCCLK0	LPCCLK1	SB_AZ_RST#	SB_GPO17, SB_GPO16 ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	IMC ENABLED	CLKGEN ENABLED (Use Internal)	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	DISABLE PCI ROM BOOT DEFAULT	DEFAULT, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

Main Source

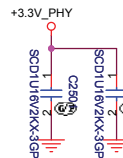


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **ATI-SB700_STRAPPING_(5/5)**

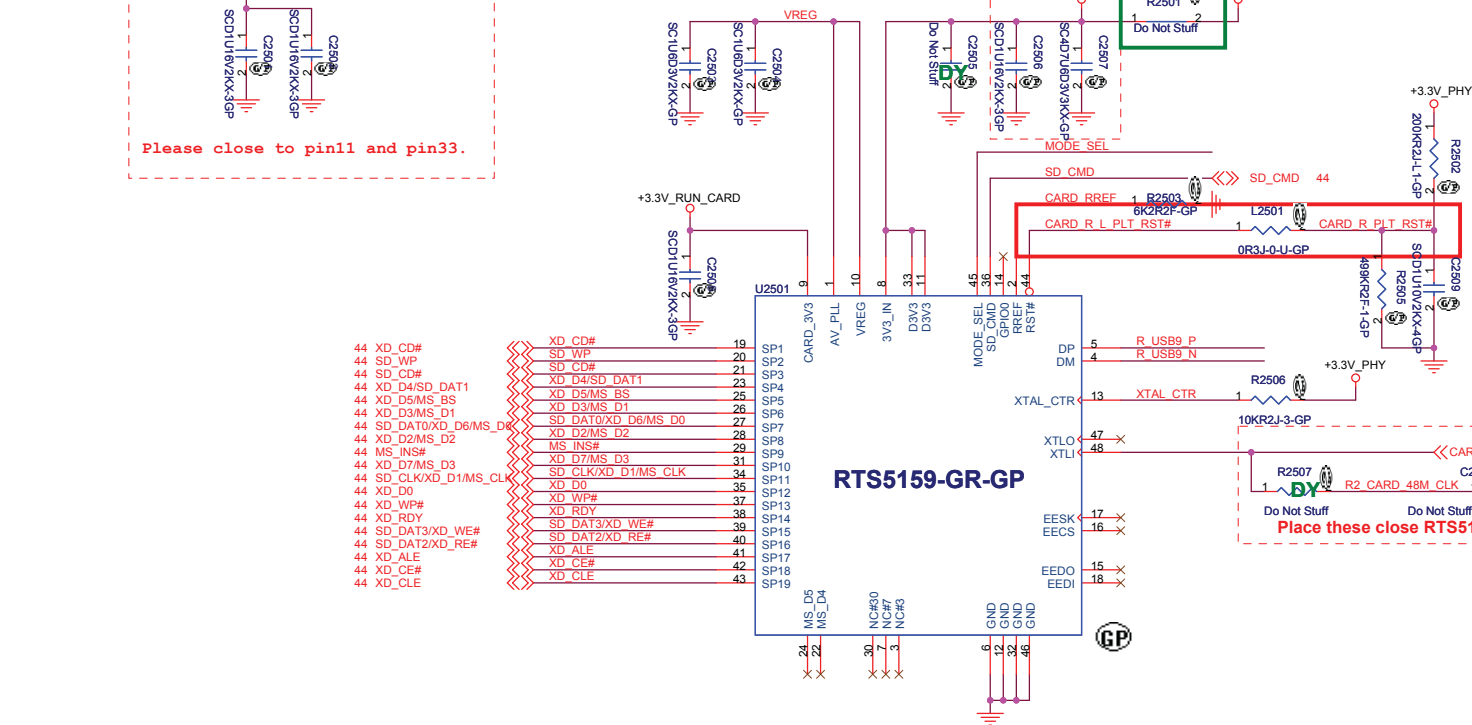
Size A3	Document Number Riya Discrete	Rev A00
Date Wednesday, August 26, 2009	Sheet 22	of 65

SSID = SDIO



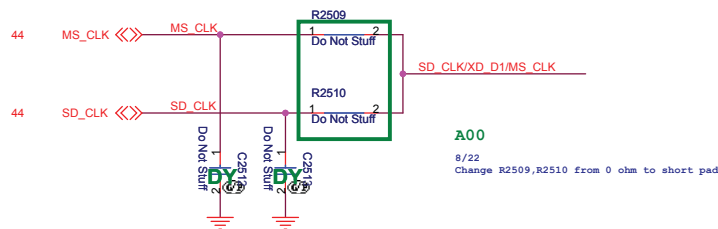
Please close to pin11 and pin33.

Please close to pin8.

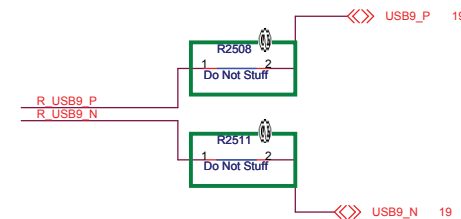


X01
04/08 Del
1. Del R2504, C2510, R1817

A00
8/24
Change R2501, R2508, R2511, R2512 from 0 ohm to short pad
8/26
Del L2502

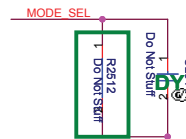


A00
8/22
Change R2509, R2510 from 0 ohm to short pad



Power mode select

No staff R and C for power saving mode.

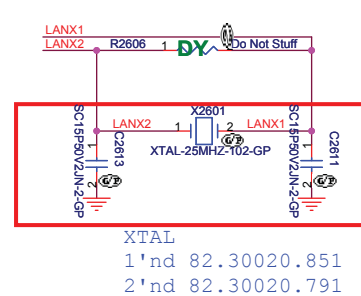
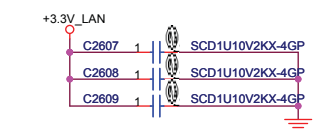
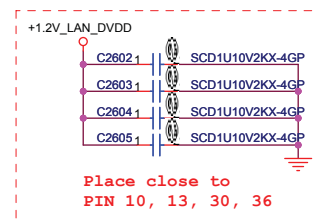
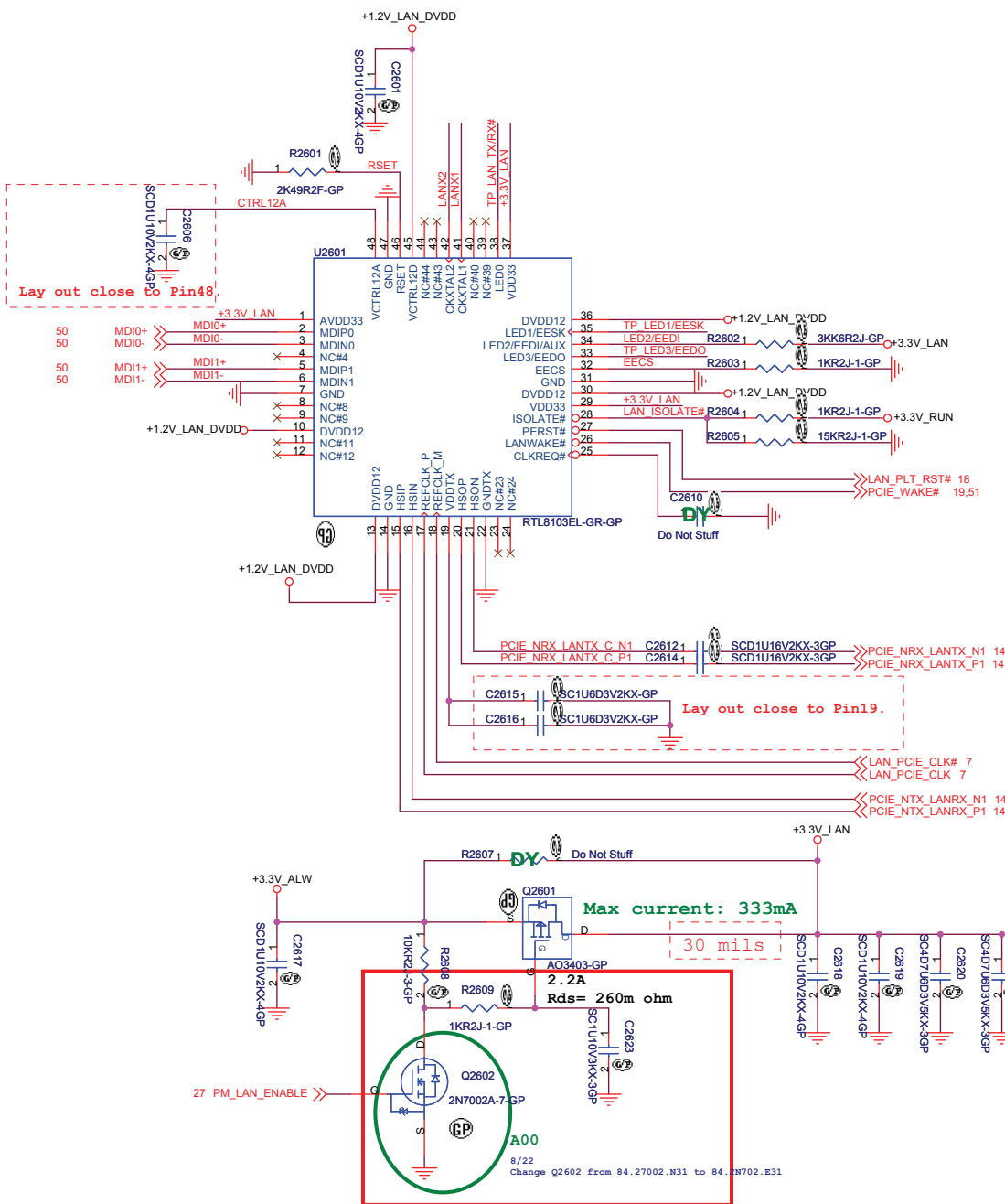


Main Source

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Card Reader Realtek RTS5159			
Size	Document Number	Rev	
Custom	Riya Discrete	A00	
Date:	Wednesday, August 26, 2009	Sheet	25 of 65

www.vinafix.vn

SSID = LOM



X01
04/06 modify
1. Change C2611/C2613 from 18P to 15P

TP2601 1 TP LED3/EED0
TP2602 1 TP LED1/EESK
TP2603 1 TP LAN_TX/RX#

www.vinafix.vn

SSID = KBC

KBC_SHBM	SHBM
1 (EMPTY R2713)	Disables
*0 (STUFF R2713)	Enable

*DEFAULT

SB TYPE	D2704	R2734	R2735
*SB700	STUFF	STUFF	EMPTY
SB710	EMPTY	EMPTY	STUFF

*DEFAULT

MB VERSION ID			
	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
*-1	0	1	1

*DEFAULT

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

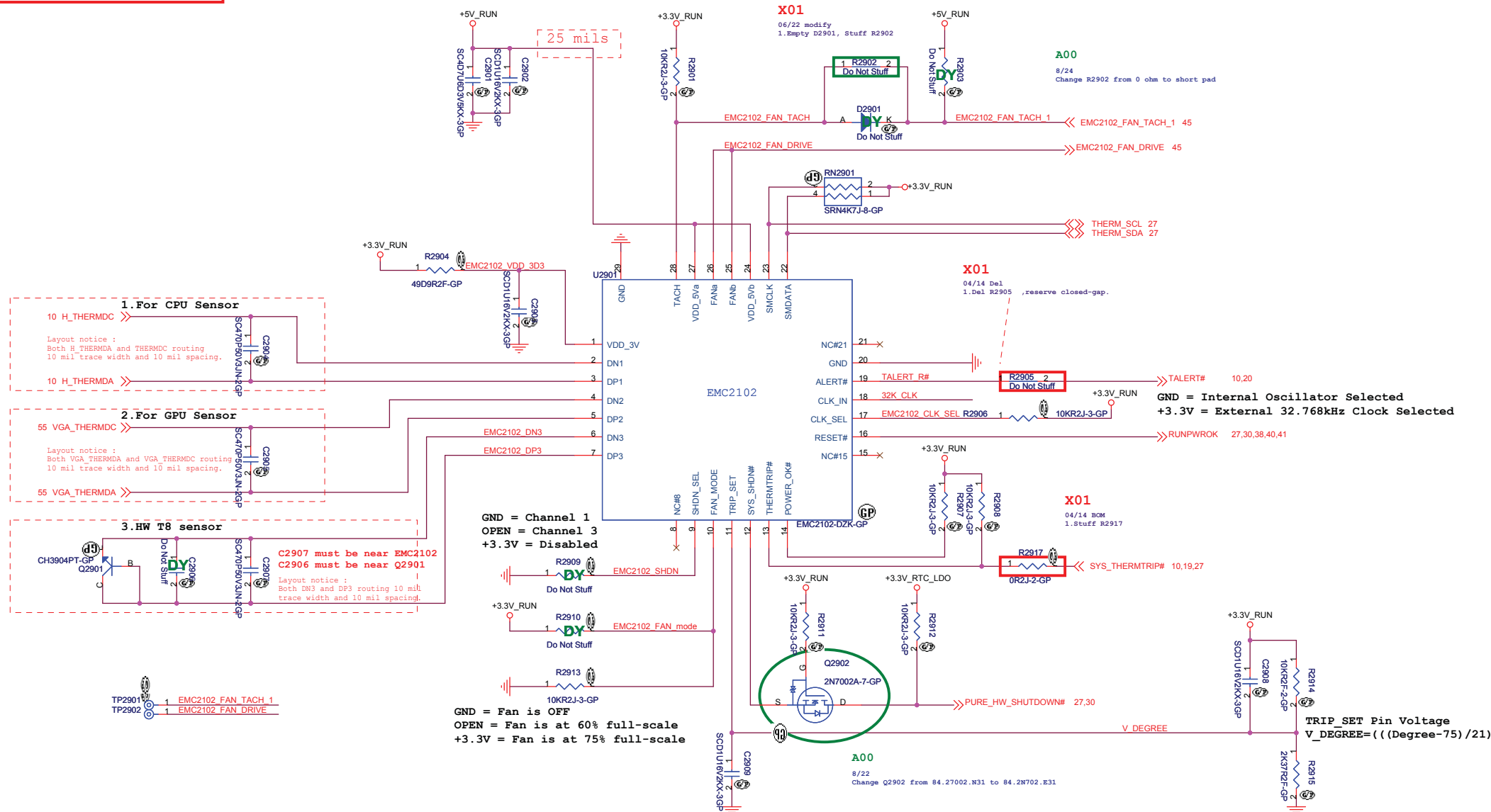
Title: **KBC WPCE773L**

Size: Custom Document Number: **Riya Discrete** Rev: **A00**

Date: Wednesday, September 09, 2009 Sheet 27 of 65

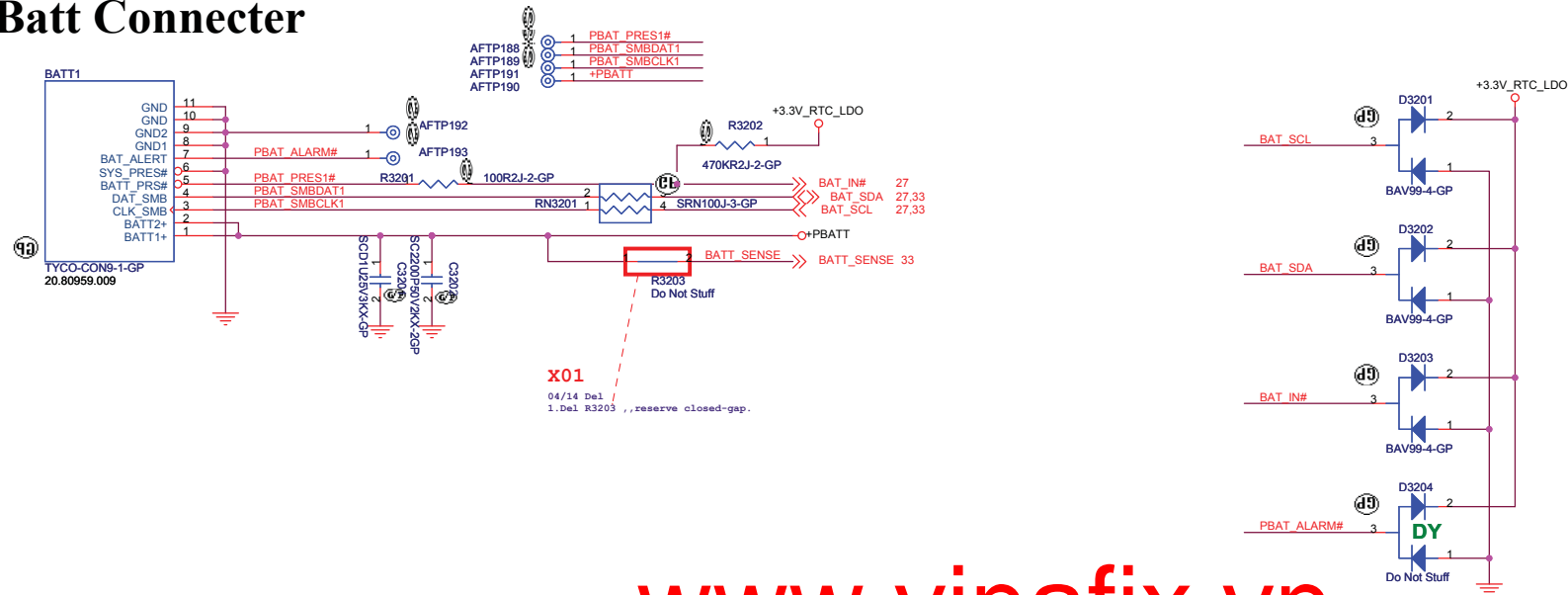
www.vinafix.vn

SSID = Thermal



(Blanking)

Batt Connector

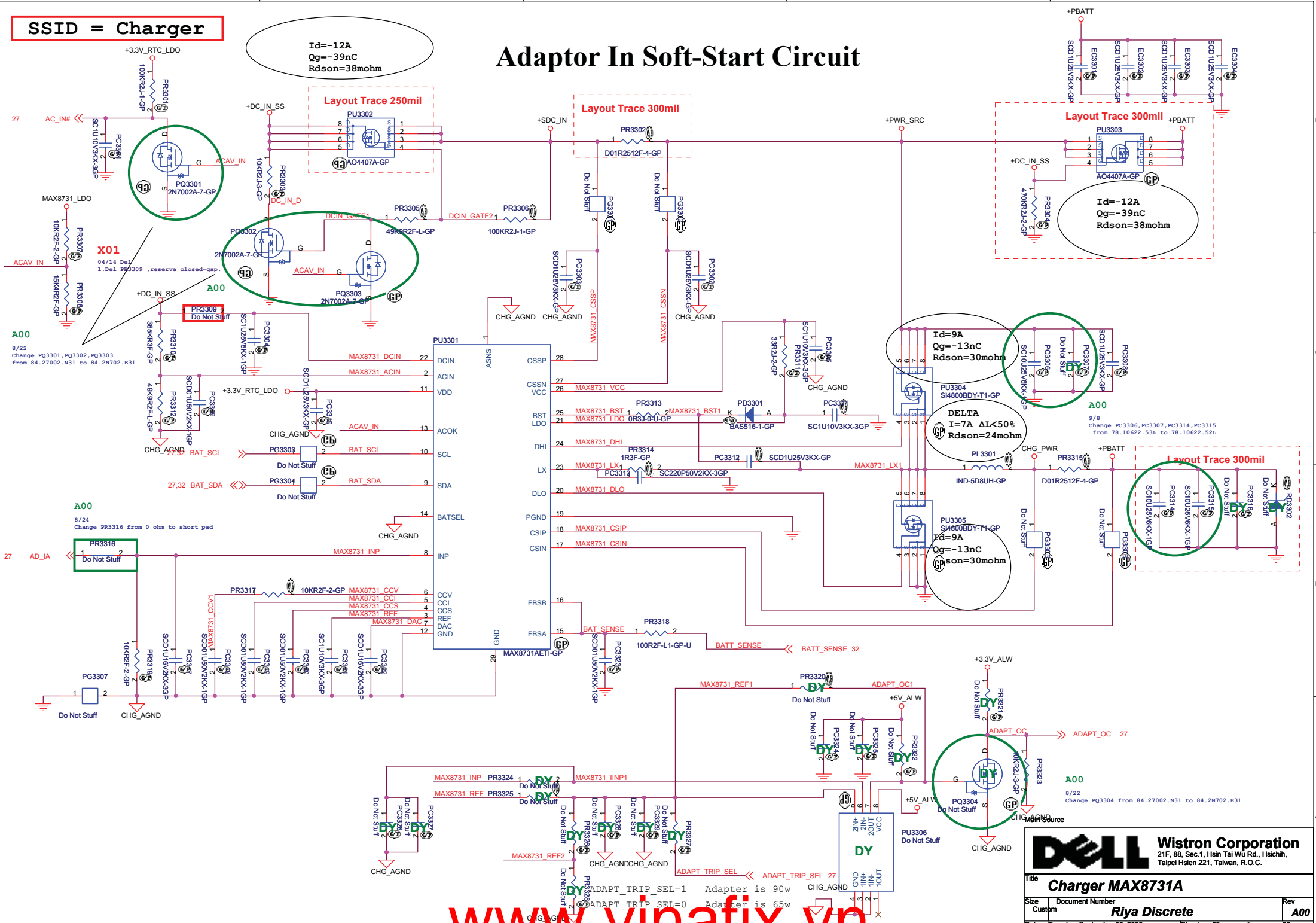


Main Source

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DC IN/BATT CONN			
Size	Document Number	Rev	
Custom	Riya Discrete	A00	
Date:	Wednesday, August 26, 2009	Sheet	32 of 65

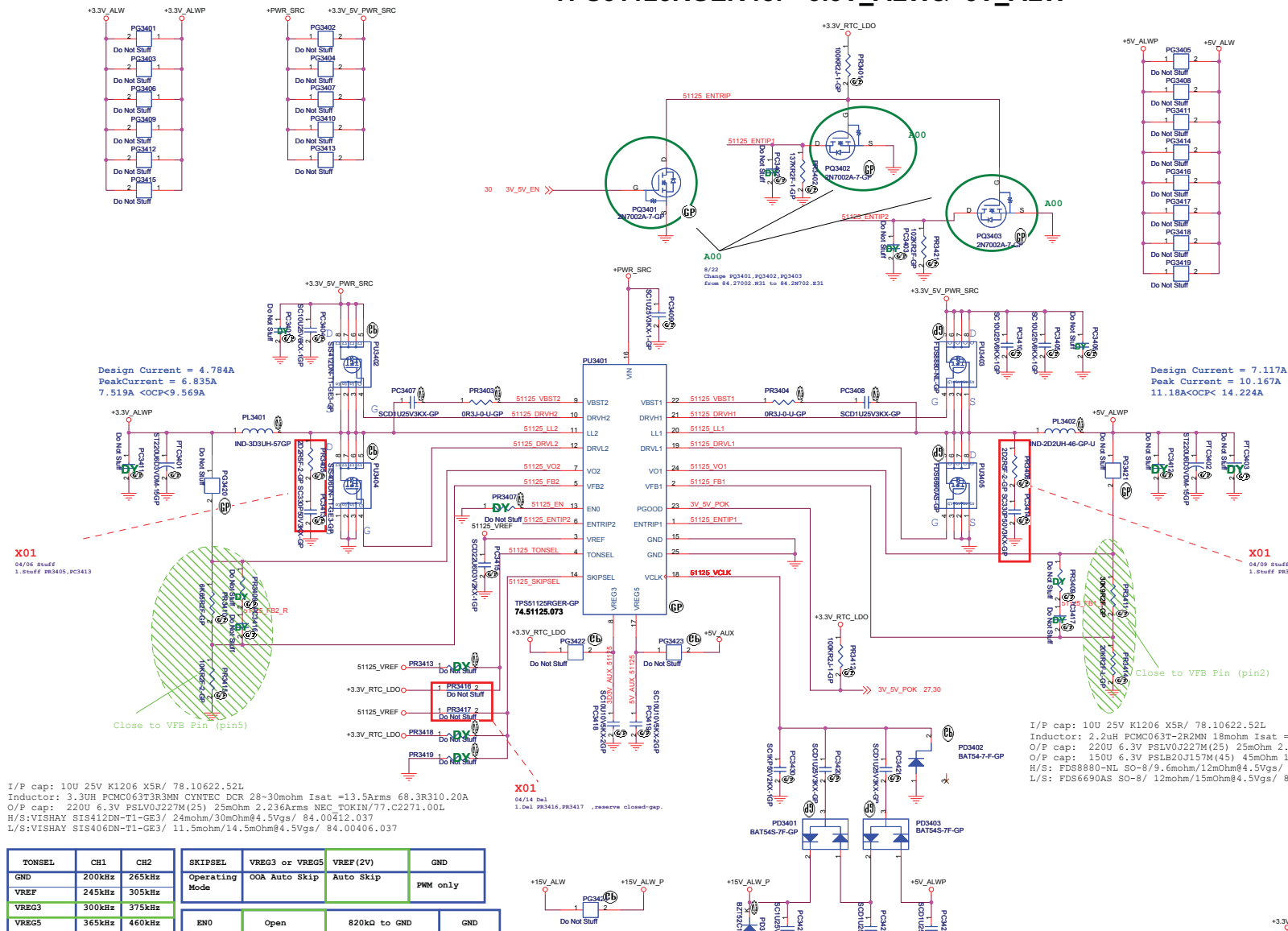
SSID = Charger

Adaptor In Soft-Start Circuit

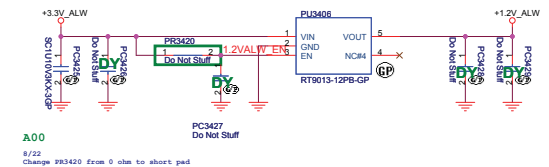


SSID = PWR.Plane.Regulator_3p3v5v

TPS51125RGER for +3.3V_ALW&+5V_ALW



RT9013 for +1.2V_ALW

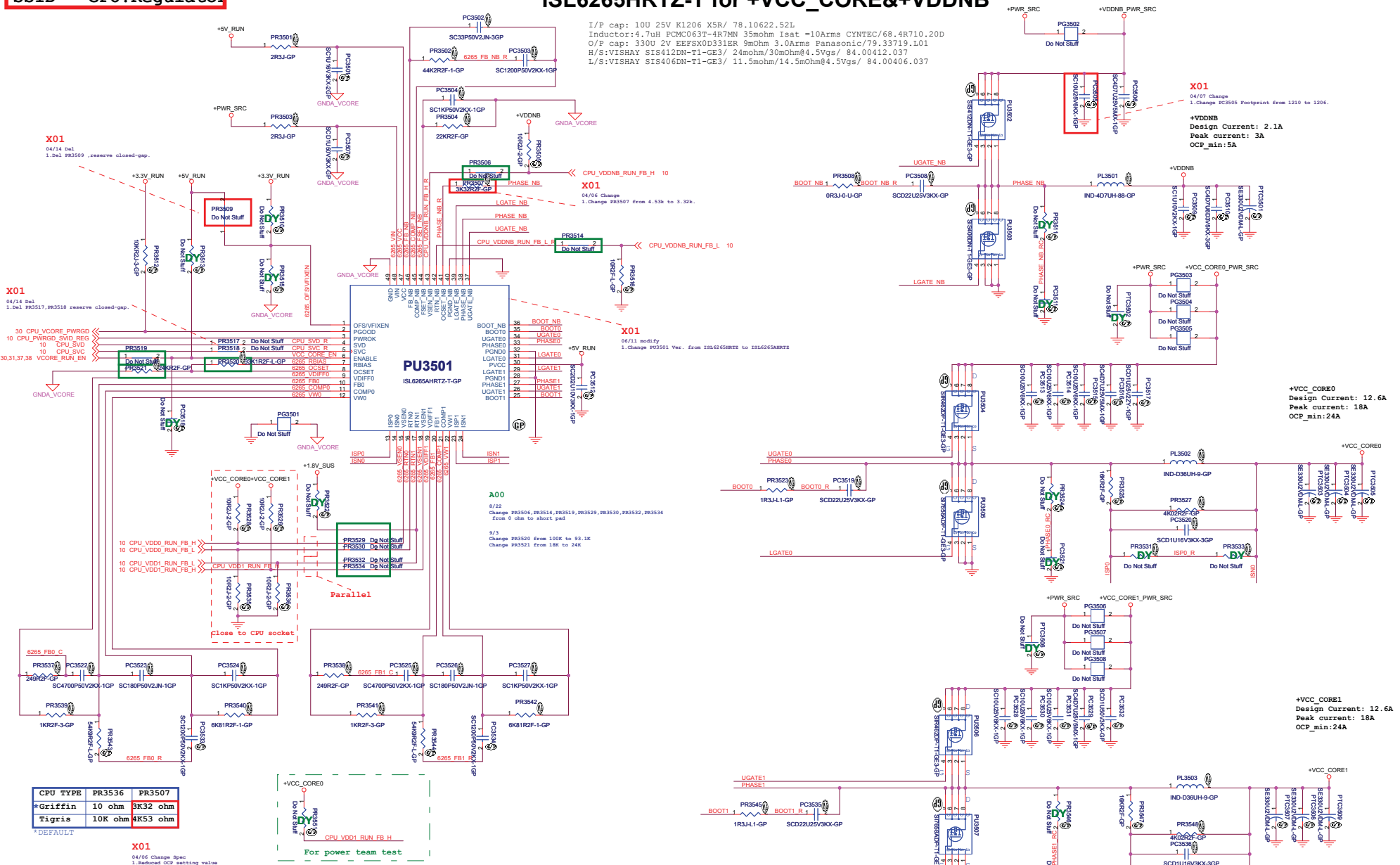


Main Source

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D31ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: VISHAY SIS406DN-T1-GE3/ 11.5mohm/14.5mOhm@4.5Vgs/ 84.00406.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36uH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D31ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: VISHAY SIR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
L/S: VISHAY SI7658ADP/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

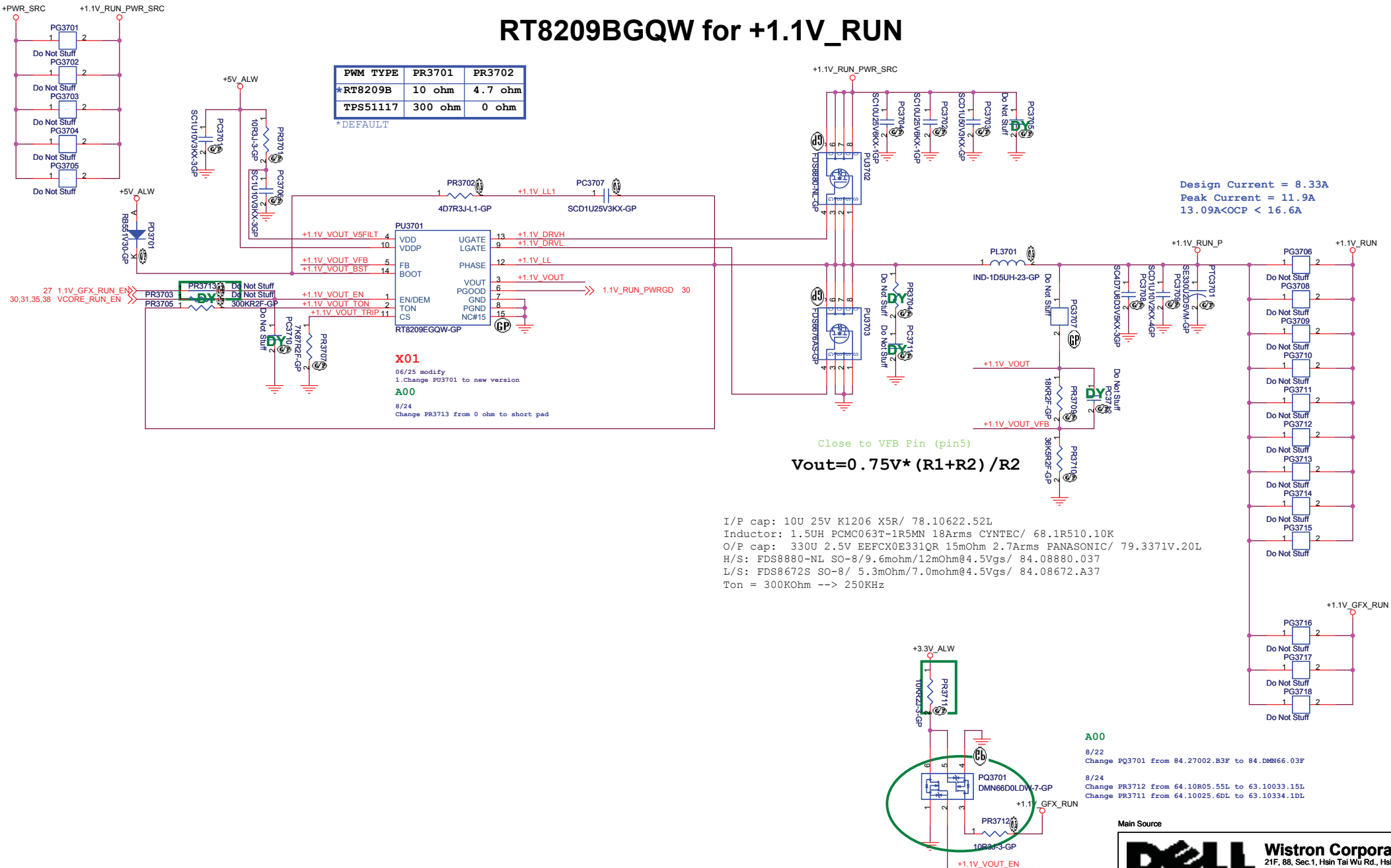
Main Source

SSID = PWR.Plane.Regulator_+1.1V_RUN

RT8209BGQW for +1.1V_RUN

PWM TYPE	PR3701	PR3702
*RT8209B	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT

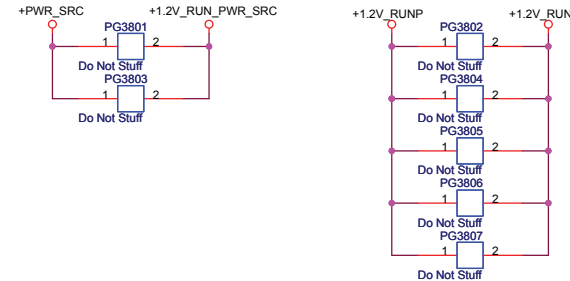


Main Source

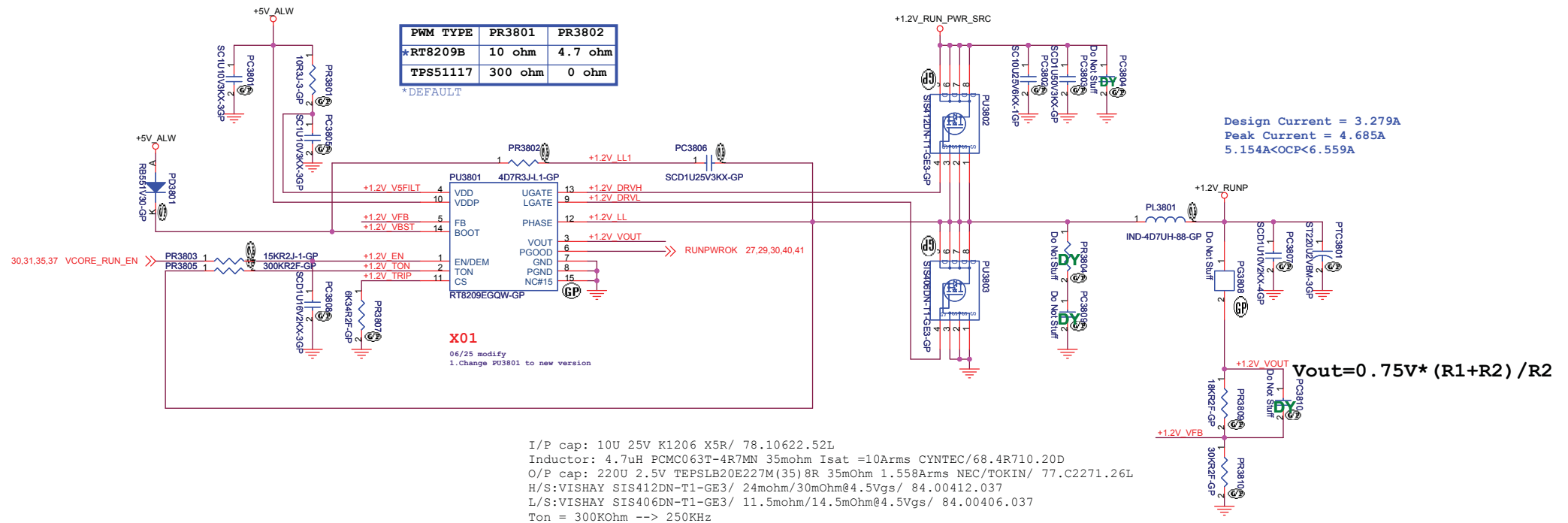
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title VREG : +1.1V_RUN			
Size	Document Number	Rev	
Custom	Riya Discrete	A00	
Date: Wednesday, August 26, 2009	Sheet 37	of	65

www.vinafix.vn

SSID = PWR.Plane.Regulator_+1.2V_RUN



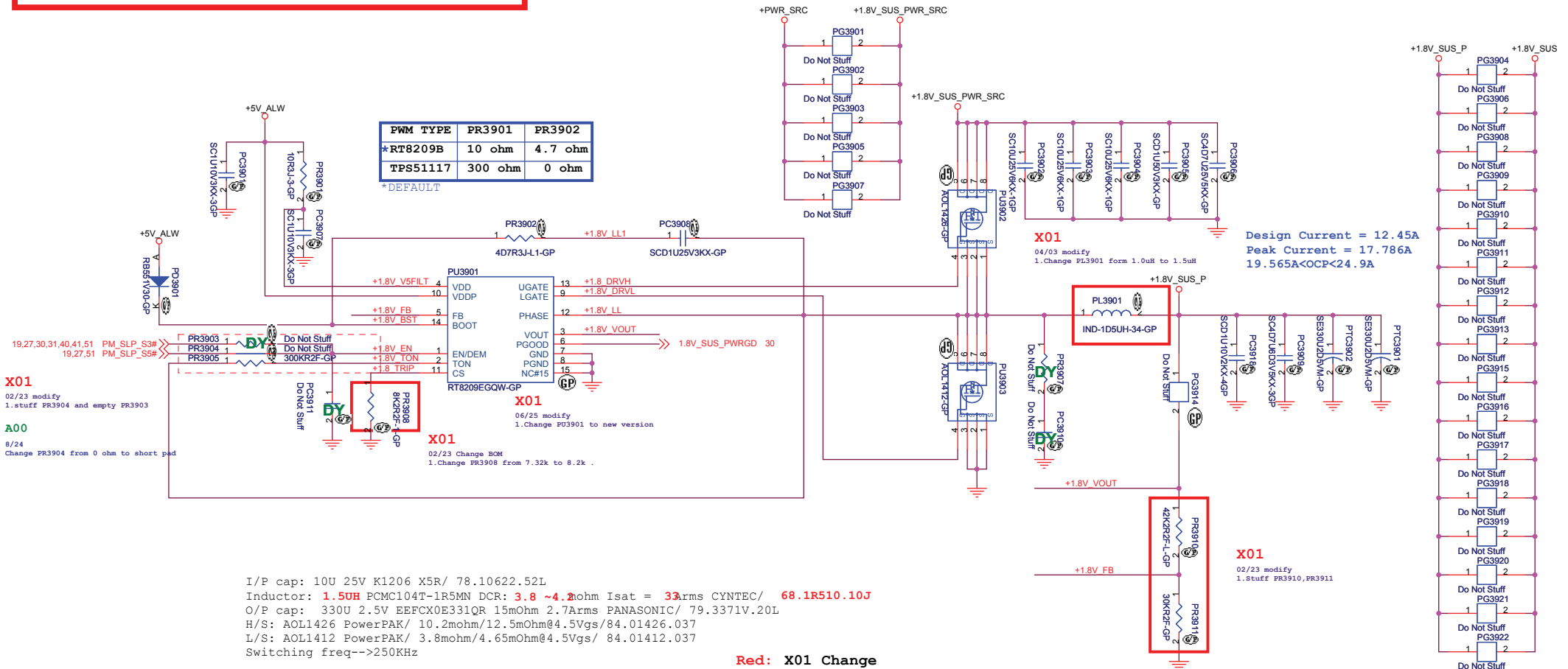
RT8209BGQW for +1.2V_RUN



www.vinafix.vn

SSID = PWR.Plane.Regulator_+1.8V

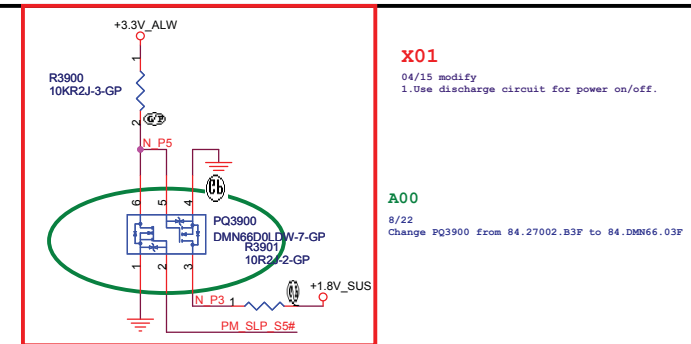
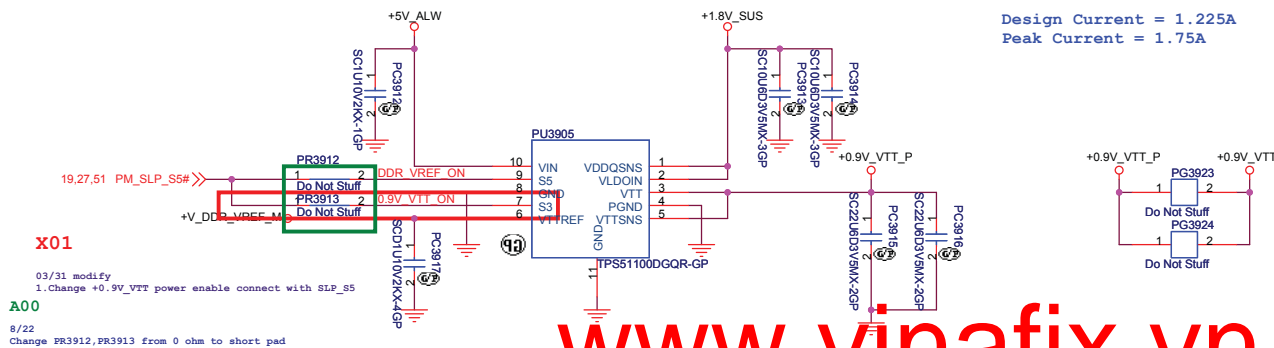
RT8209BGQW for +1.8V_SUS



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN DCR: 3.8 ~4.2ohm Isat = 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037
Switching freq-->250KHz

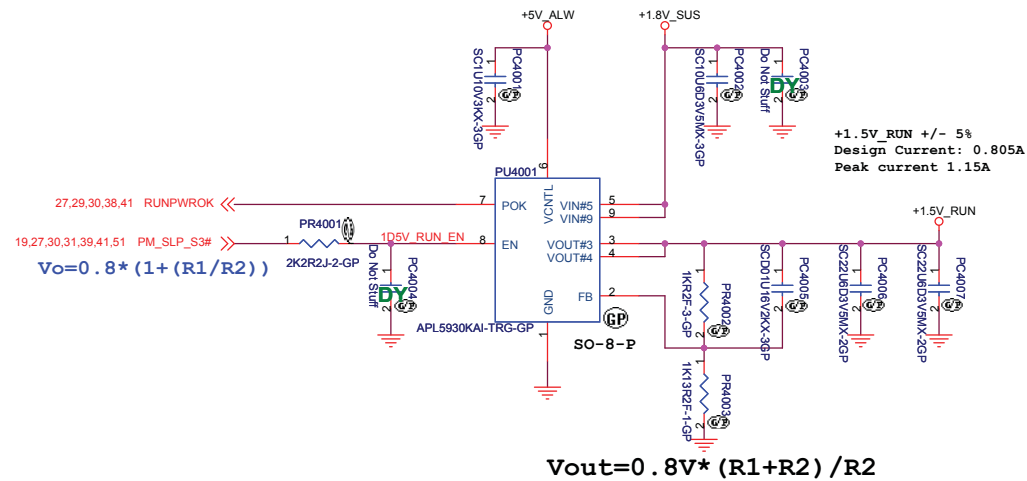
SSID = PWR.Plane.Regulator_+0.9V

TPS51100 for +0.9V_VTT



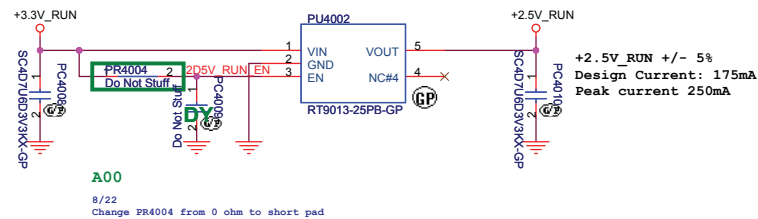
SSID = PWR.Plane.Regulator_1p5v

APL5930KAI for +1.5V_RUN



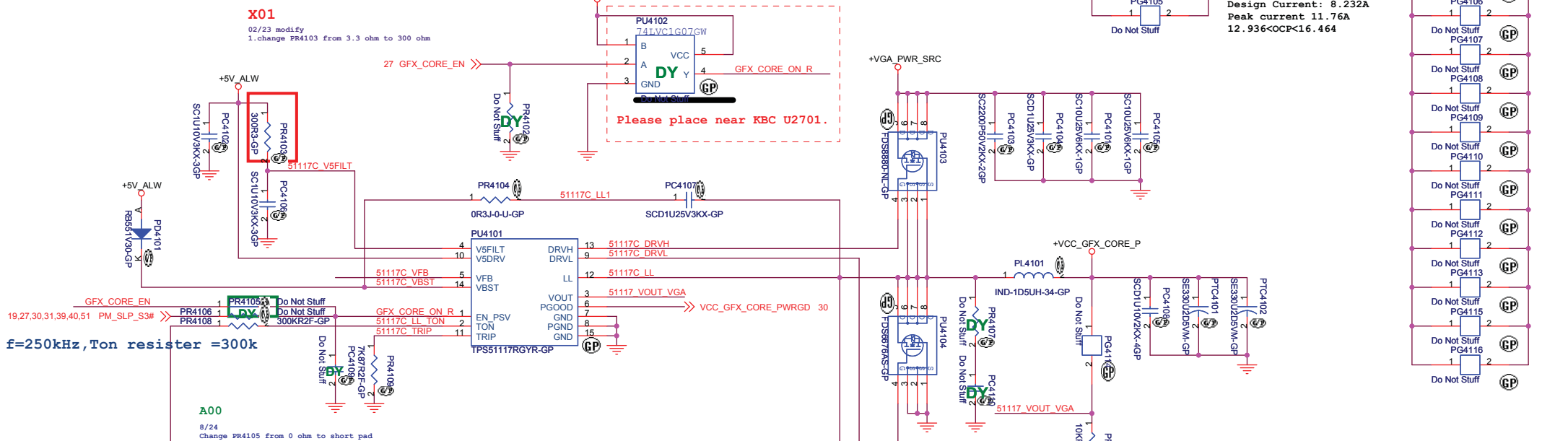
SSID = PWR.Plane.Regulator_2p5v



RT9013-25PB for +2.5V_RUN



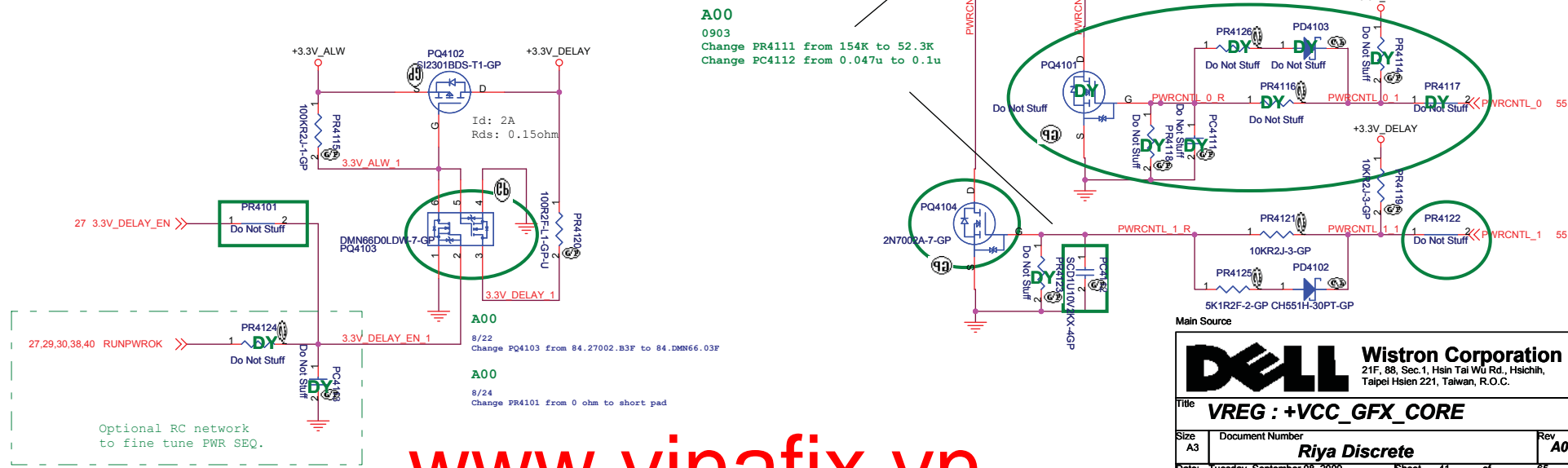
```
SSID = Video.PWR.Regulator
```

TPS51117RGYR for +VCC_GFX_CORE



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
X	H	1.05V
X	X	
X	X	
X	L	0.90V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN DCR:3.3k ~4.2mohm Isat =33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFX0E331QR 15mohm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: FDS8880-NL SO-8/9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->250KHz



Main Source

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VREG : +VCC GFX CORE
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Size A3	Document Number <i>Riya Discrete</i>	Rev A00
Date: Tuesday, September 08, 2009	Sheet 41 of 65	

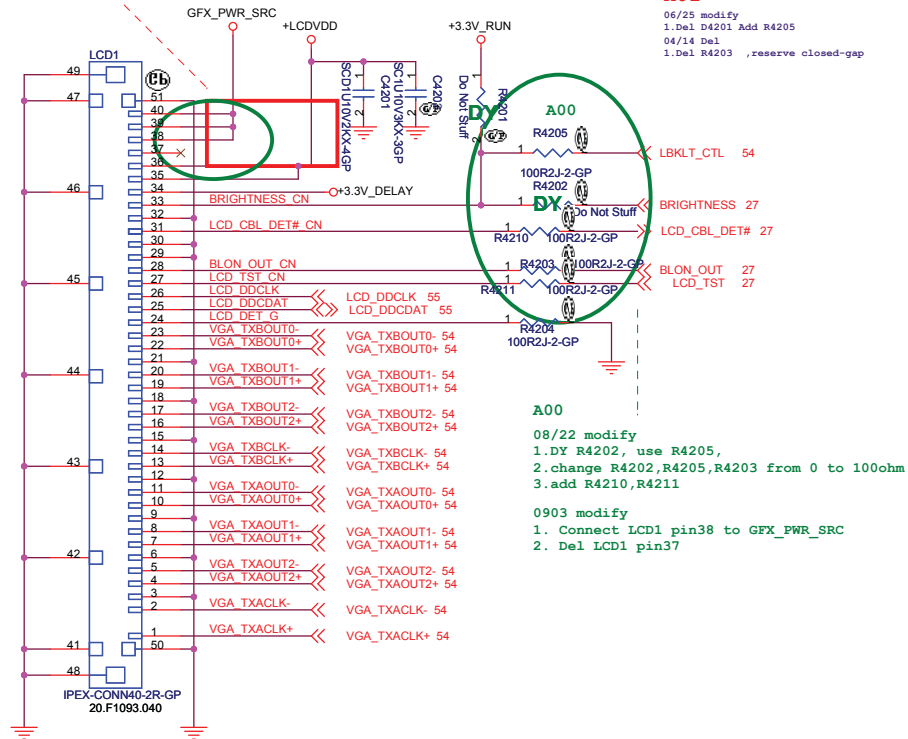
www.vinafix.vn

SSID = VIDEO

X01

- 06/09 modify
1. Connect LCD1 pin37 to +LCDVDD
2. Del LCD1 pin38

LVDS CONNECTOR



X01

- 06/25 modify
1. Del D4201 Add R4205
04/14 Del
1. Del R4203 ,reserve closed-gap

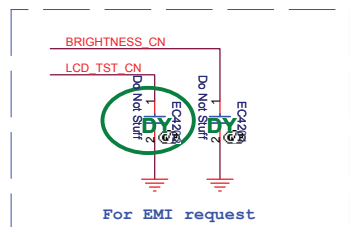
A00

- 08/22 modify
1. DY R4202, use R4205,
2. change R4202, R4205, R4203 from 0 to 100ohm
3. add R4210, R4211

- 0903 modify
1. Connect LCD1 pin38 to GFX_PWR_SRC
2. Del LCD1 pin37

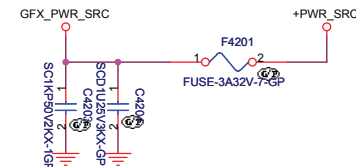
A00

- 08/27 modify
1. Chang EC4202 Pin1 from LCD_TST to LCD_TST_CN



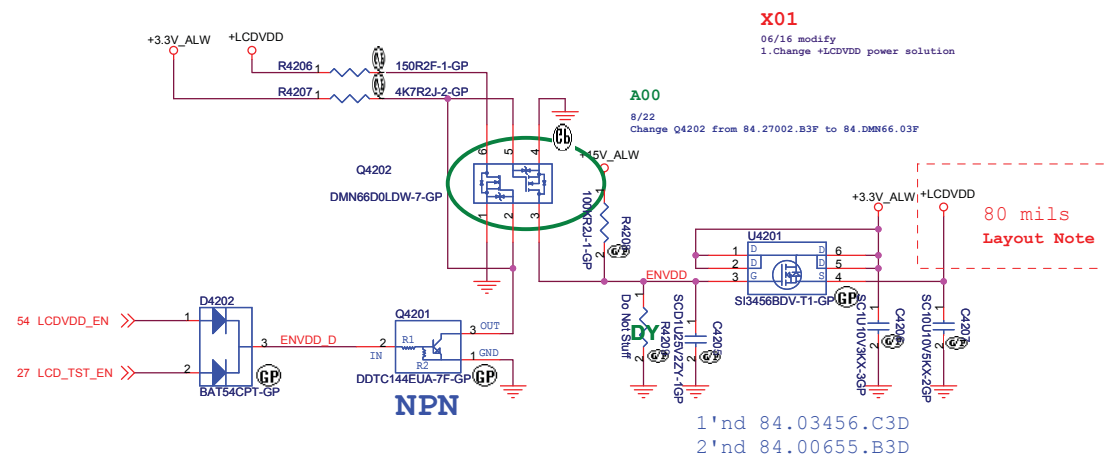
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



X01

- 06/16 modify
1. change +LCDVDD power solution

A00

- 8/22
Change Q4202 from 84.27002.B3F to 84.DMN66.03F

80 mils
Layout Note

- 1'nd 84.03456.C3D
2'nd 84.00655.B3D

Main Source

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

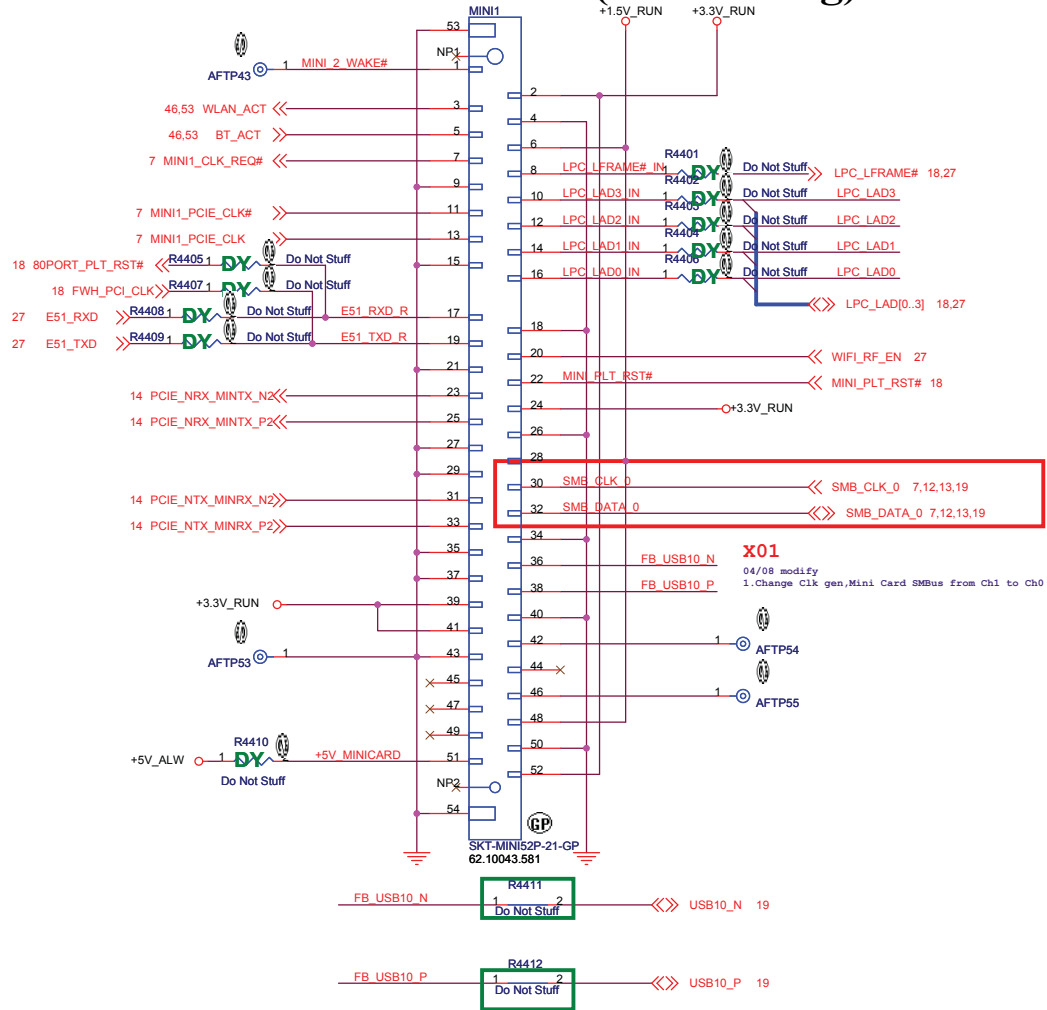
Title **LCD&Inverter CONN**

Size Custom Document Number **Riya Discrete** Rev **A00**
Date: Thursday, September 03, 2009 Sheet 42 of 65

www.vinafix.vn

SSID = Wireless

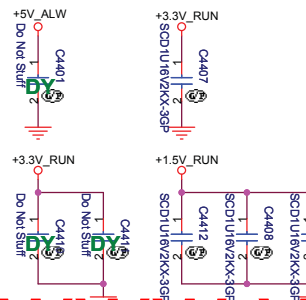
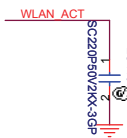
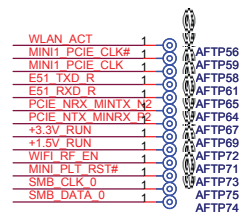
Mini Card Connector(802.11a/b/g)



A00

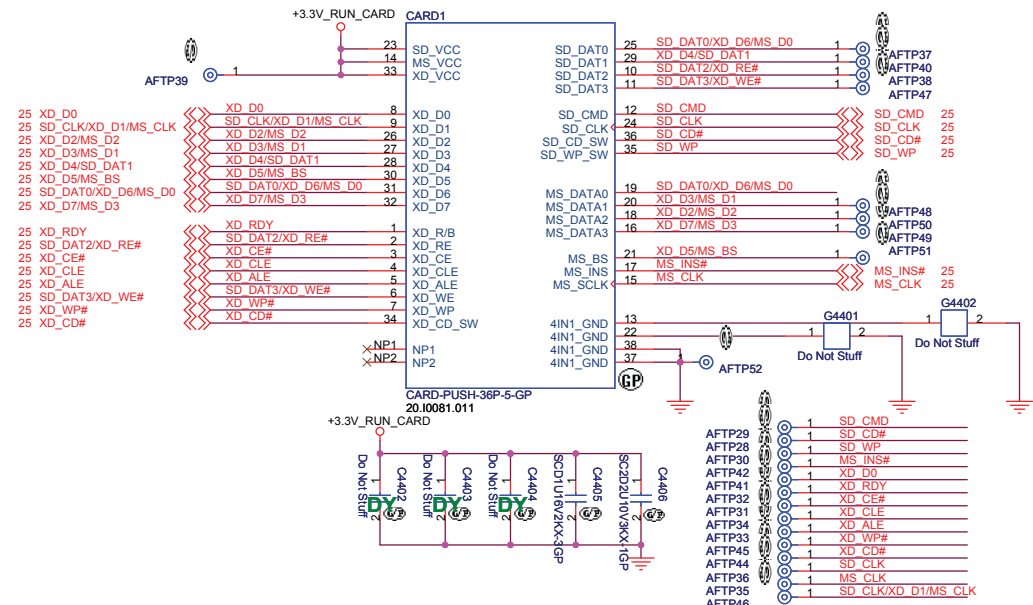
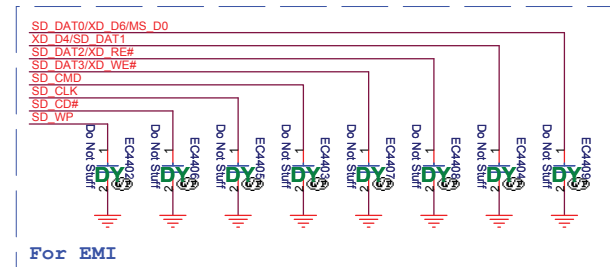
8/24
Change R4411,R4412 from 0 ohm to short pad

8/26
Del L4401



SSID = SDIO

SD/XD/MS Card Reader



Main Source



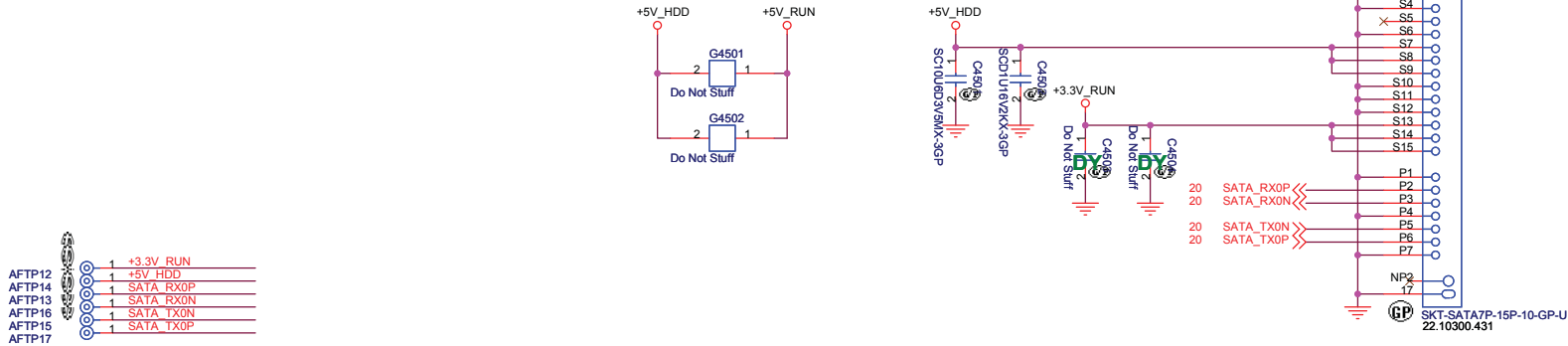
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title MiniCard&Card Reader CONN			
Size Custom	Document Number Riya Discrete	Rev A00	
Date: Wednesday, August 26, 2009		Sheet 44	of 65

www.vinafix.vn

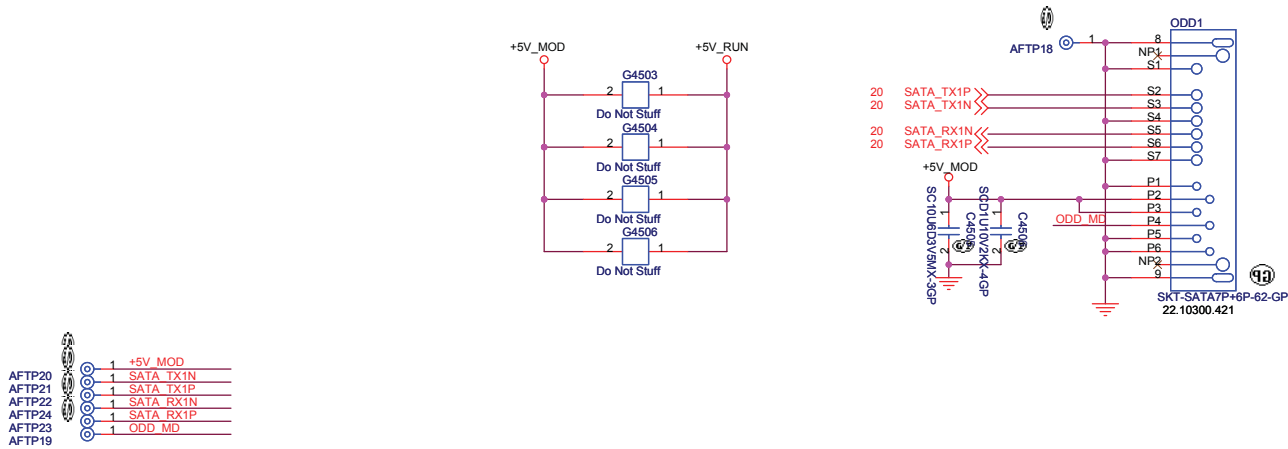
SSID = SATA

SATA HDD Connector



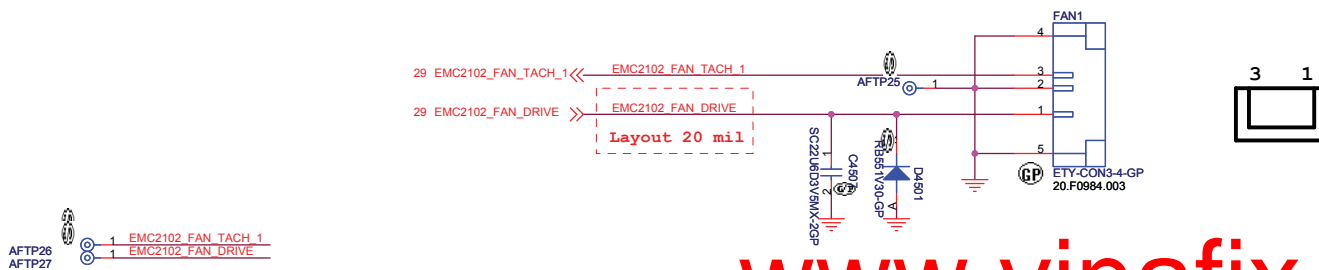
SSID = SATA

ODD Connector



SSID = Thermal

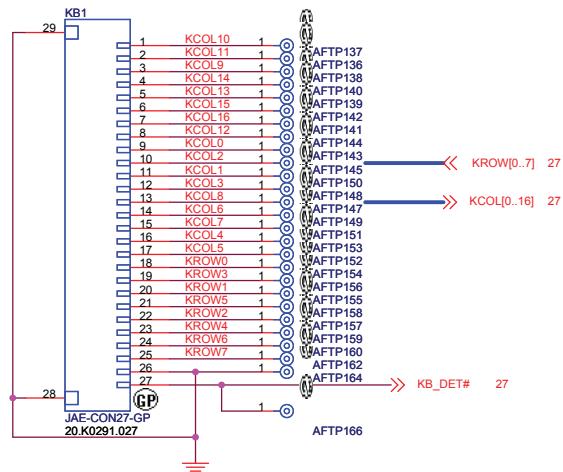
Fan Connector



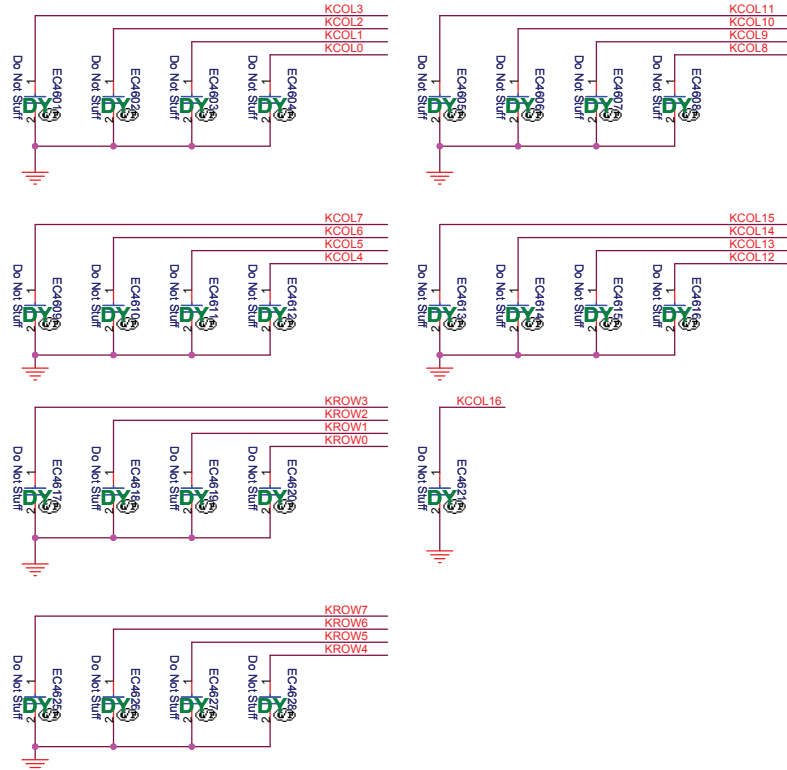
www.vinafix.vn

SSID = KBC

Internal KeyBoard Connector

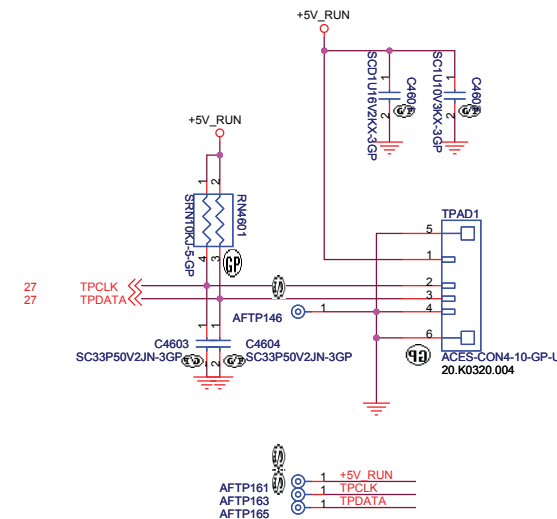


For EMI



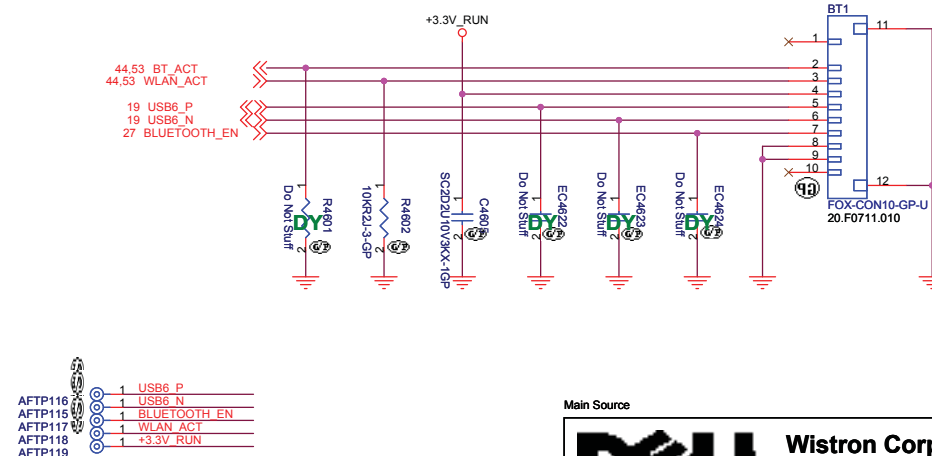
SSID = Touch.Pad

TouchPad Connector



SSID = User.Interface

Bluetooth Module conn.



Main Source

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

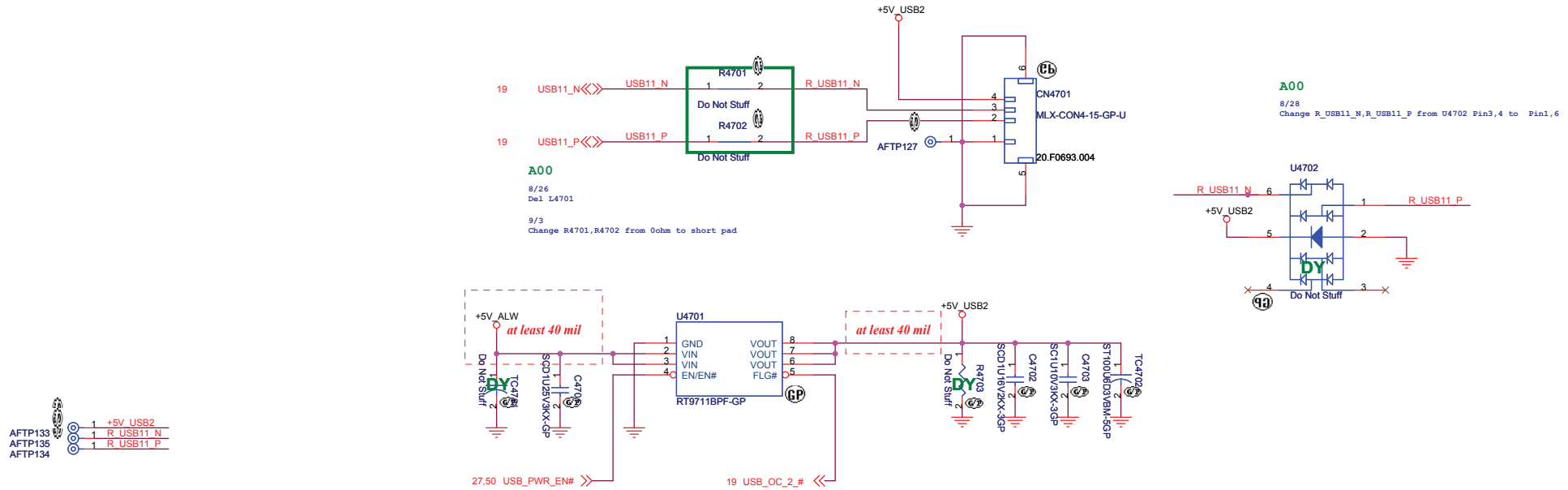
Title **KeyBoard&TouchPad&BT CONN**

Size Document Number
Custom **Riya Discrete**

Date: Wednesday, August 26, 2009 Sheet 46 of 65

SSID = USB

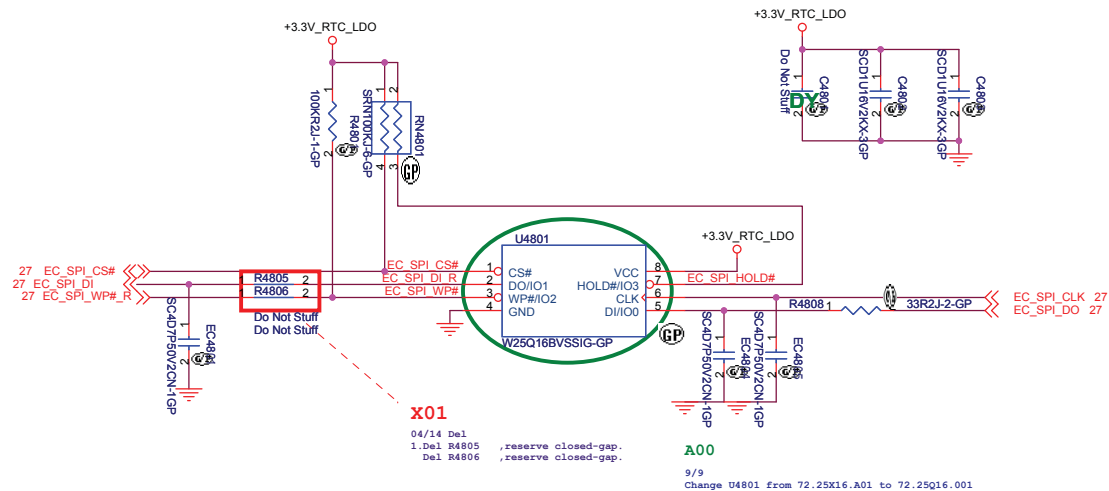
Right USB Port CONN



(Blanking)

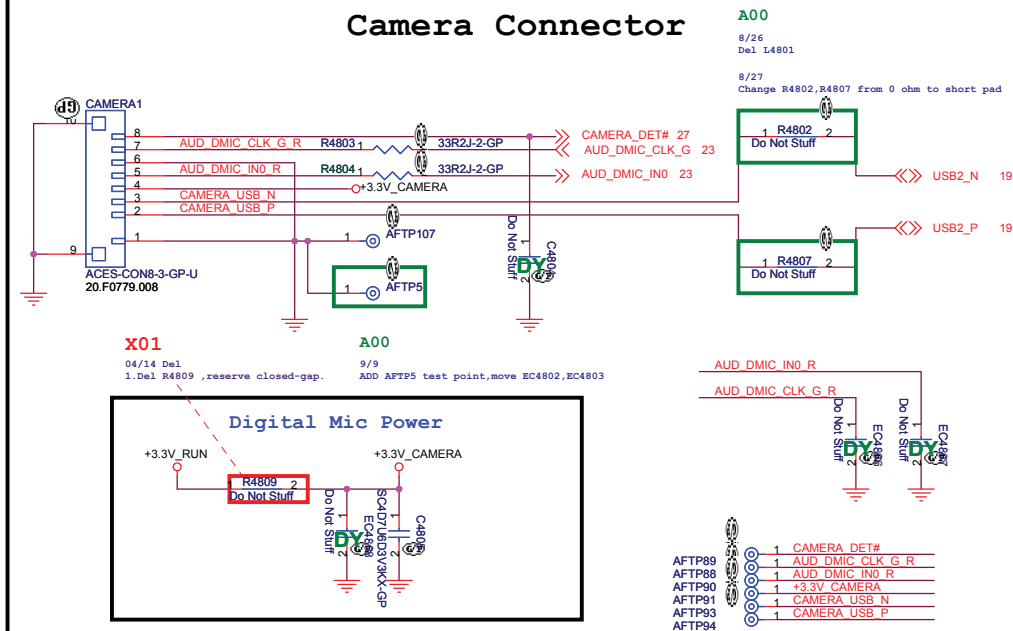
SSID = Flash.ROM

SPI FLASH ROM (16M bits)



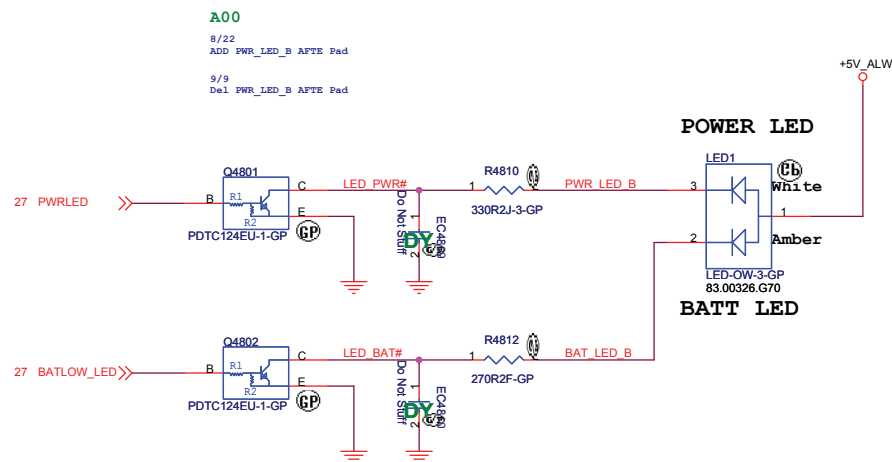
SSID = User.Interface

Camera Connector



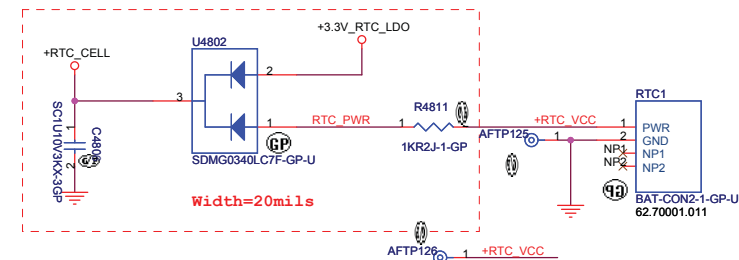
SSID = User.Interface

Power/Battery LED



SSID = RBATT

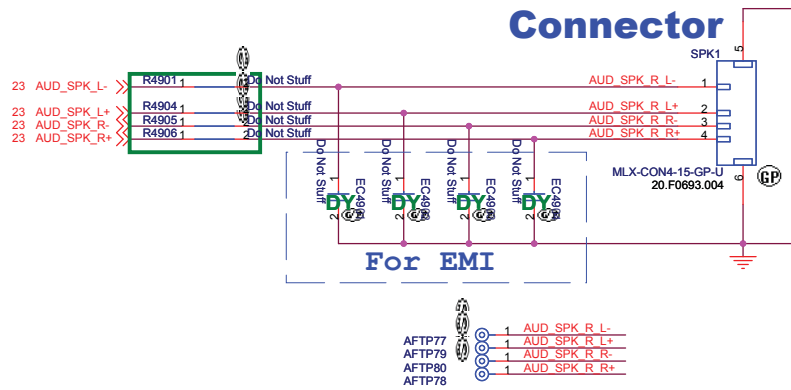
RTC Connector



www.vinafix.vn

SSID = AUDIO

Speaker Connector

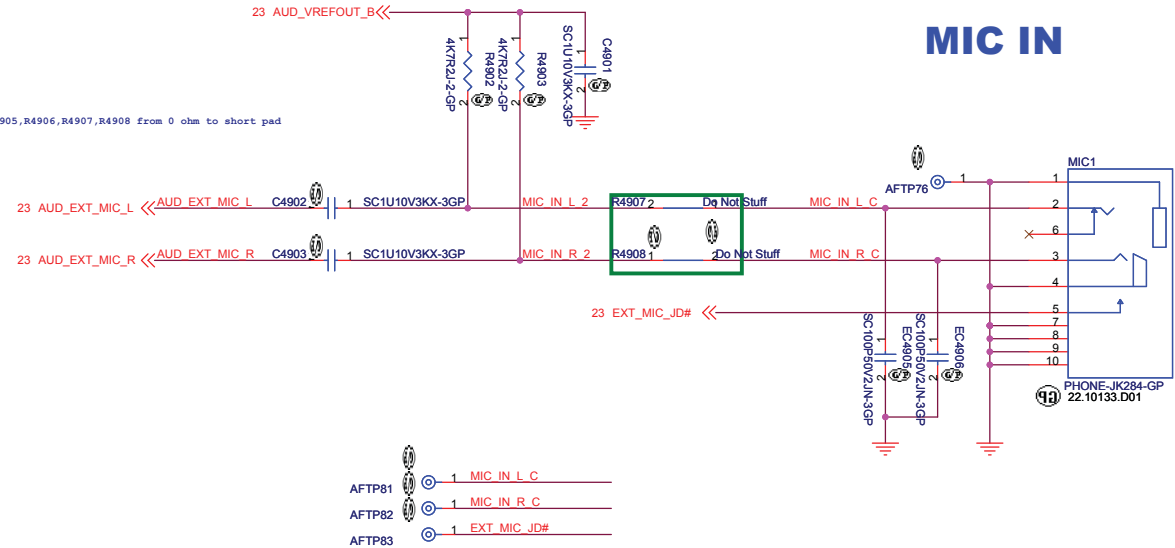


A00

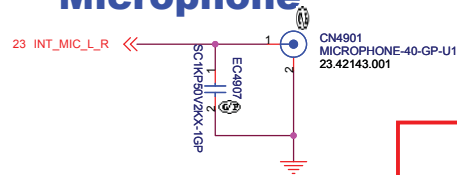
8/24

Change R4901,R4904,R4905,R4906,R4907,R4908 from 0 ohm to short pad

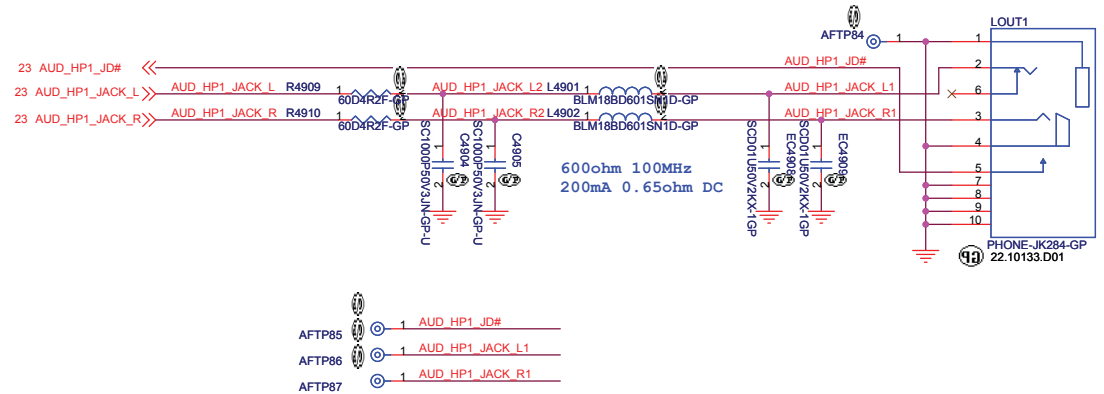
MIC IN



Internal Microphone

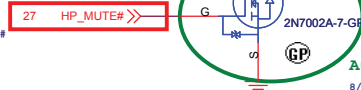


LINE1 OUT



X01

04/14 Change
1.Change netname from HP_MUTE to HP_MUTE#



X01

03/31 modify
1.Use low RDS(on) MOSFET on audio de-pop circuit

A00

8/22

Change Q4903 from 84.27002.N31 to 84.2N702.E31

9/8

DY Q4903,Q4904,Q4905,Q4906,Q4907,R4911

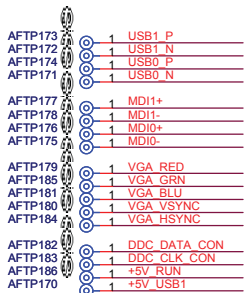
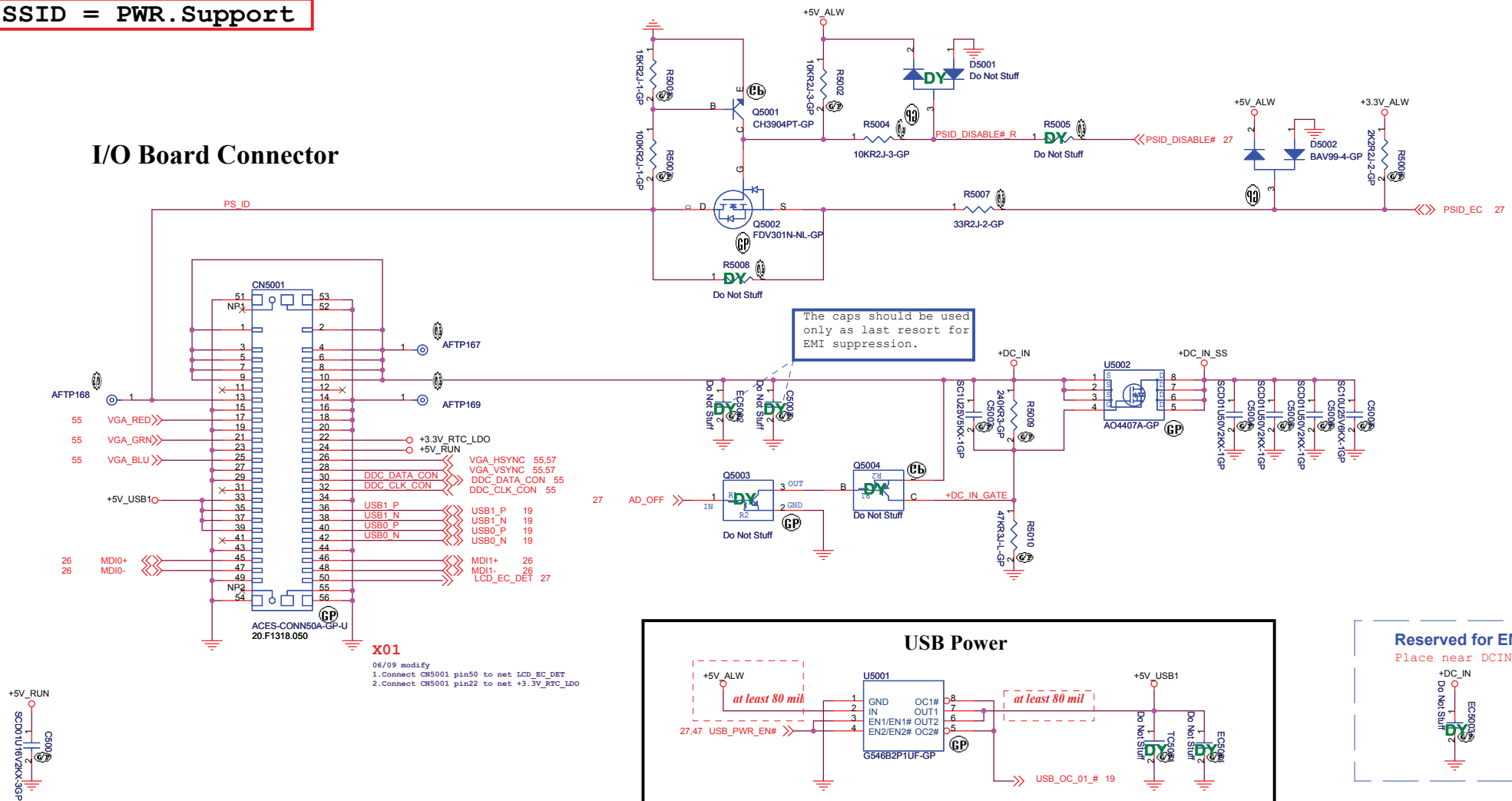
Main Source

DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Audio Jack			
Size	Document Number	Rev	
Custom	Riya Discrete	A00	
Date:	Wednesday, September 09, 2009	Sheet	49 of 65

www.vinafix.vn

SSID = PWR.Support

I/O Board Connector



www.vinafix.vn

Main Source

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

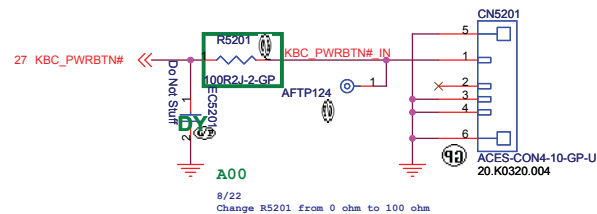
Title	IO BOARD CONN
-------	----------------------

Size Custom	Document Number <i>Riya Discrete</i>	Rev A00
Date: Wednesday, August 26, 2009	Sheet 50 of 65	

(Blanking)

SSID = User.Interface

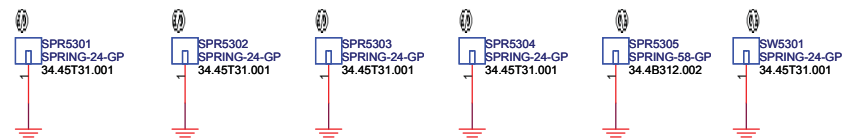
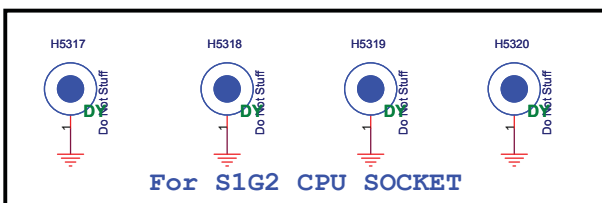
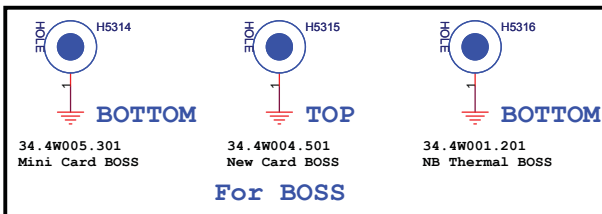
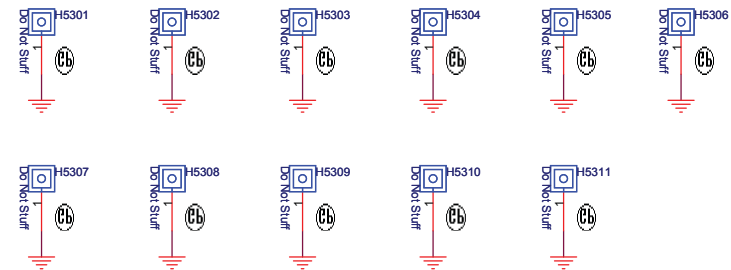
Power Board to Board CONN



(Blanking)

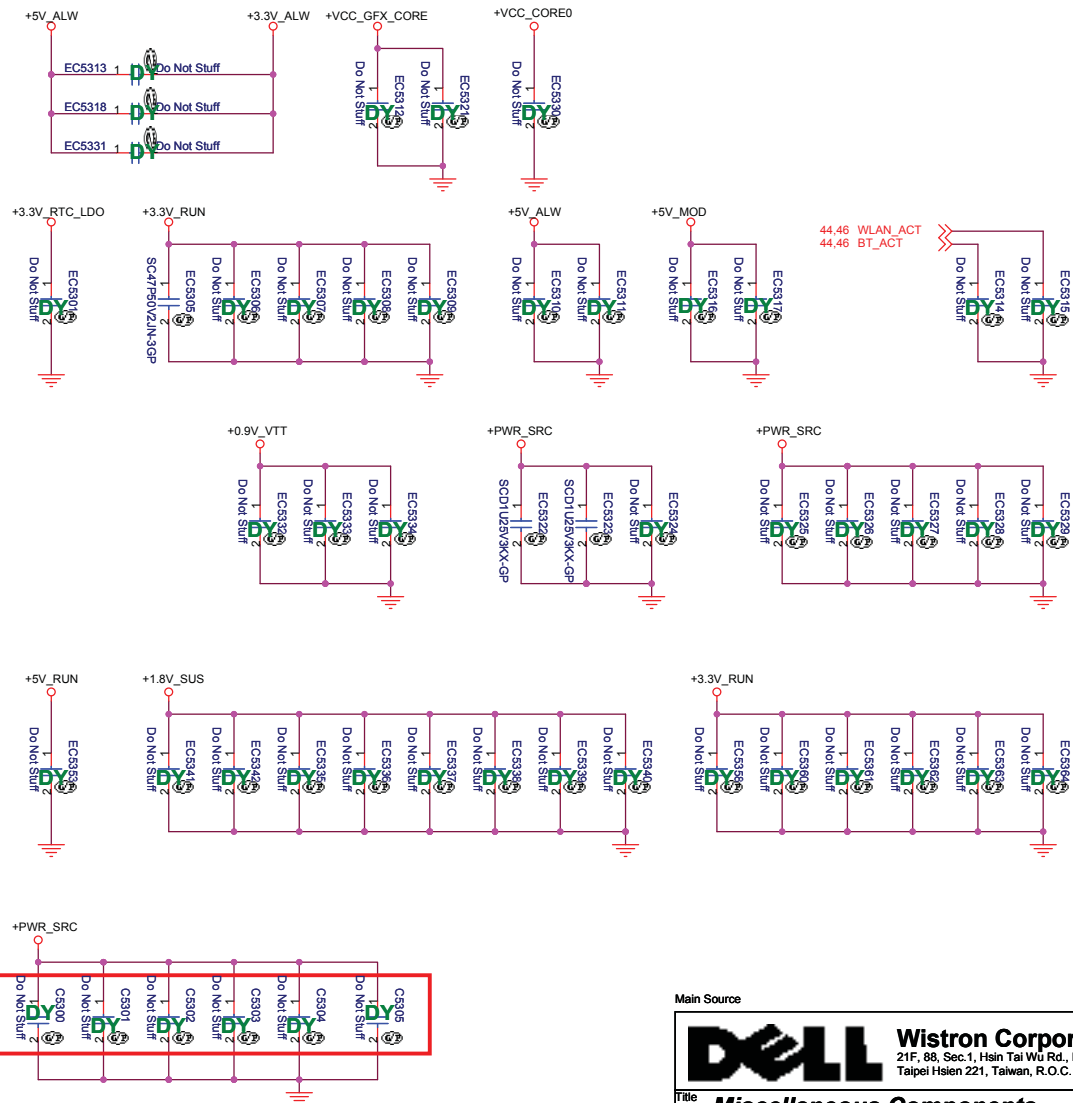
SSID = Mechanical

For EMI



x01

04/16 Add
1.Add C5300,C5301,C5302,C5303,C5304,C5305



Main Source

DELI

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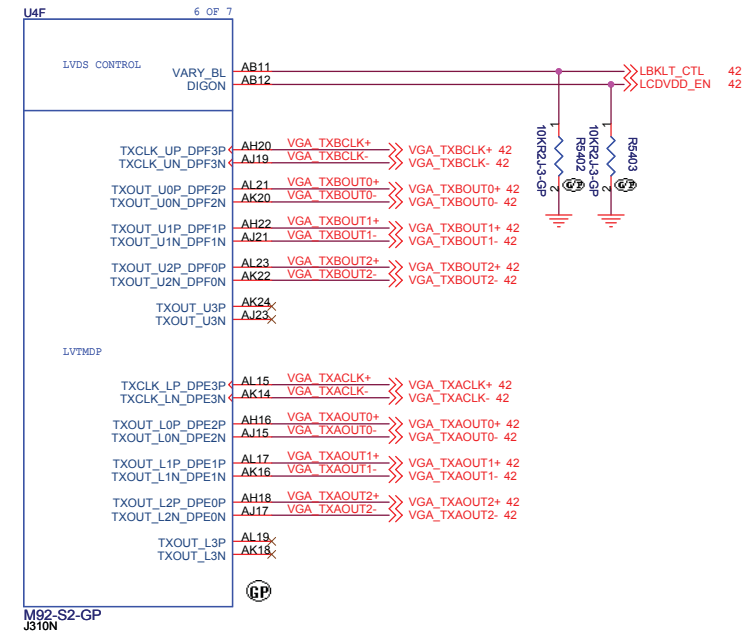
Title	Miscellaneous Components
-------	---------------------------------

Size Custom	Document Number Riya Discrete	Rev A00
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Date: Wednesday, August 26, 2009 Sheet 53 of 65

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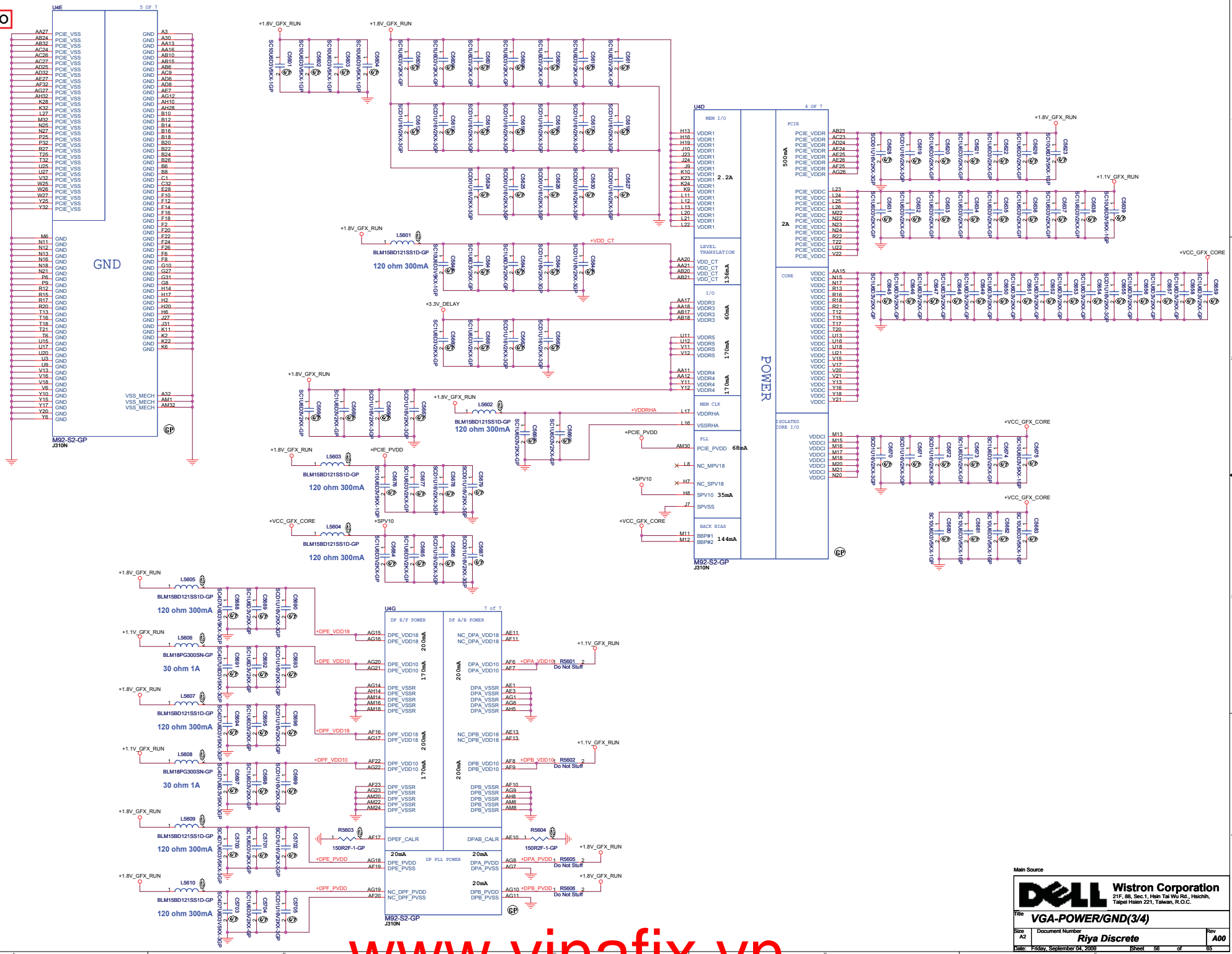
M92LP-S2 A12 : J310N



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VGA-PCIE/LVDS(1/4)			
Title			
Size Custom	Document Number Riya Discrete		Rev A01
Date:	Wednesday, August 26, 2009	Sheet 54 of 65	

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SSID = VIDEO



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Title VGA-POWER/GND(3/4)			
Size A2	Document Number Riya Discrete	Rev A00	
Date: Friday, September 04, 2009	Sheet 58	of 85	

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SSID = VIDEO

58,59 MDA[0..63]

U4C

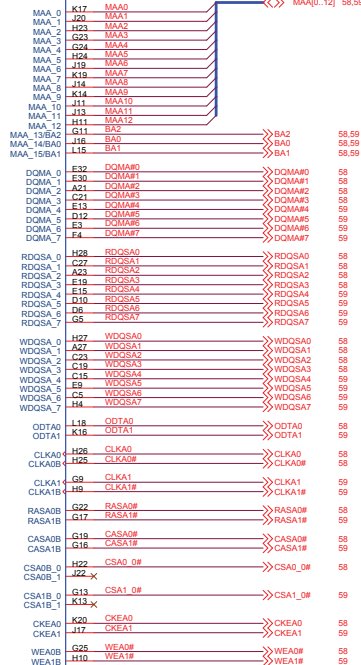
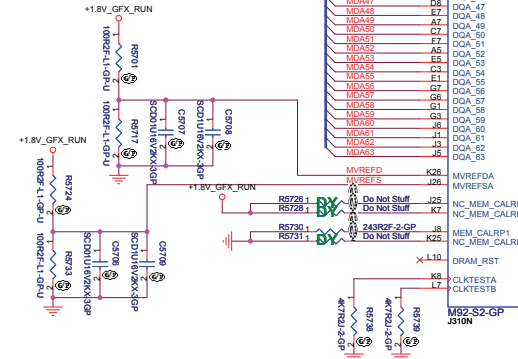
3 OF 7

MEMORY INTERFACE

VRAM TYPE	R5701	R5724
* DDR2	100R	
DDR3	40.2R	

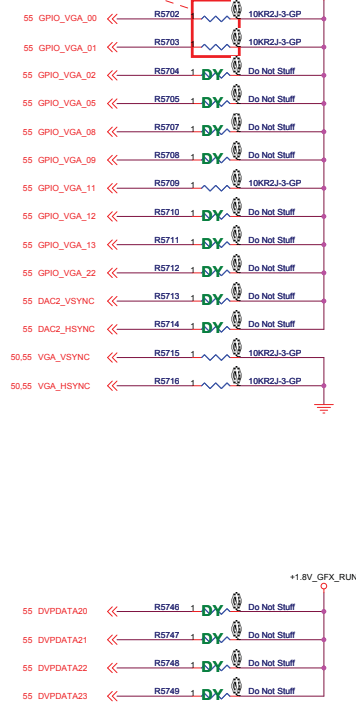
*DEFAULT

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)



X01

04/10 modify
1. Stuff R5702, R5703



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO3, H2SYNC, V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	x100
256MB	x001		M25P10A	x101
64MB	x010		M25P20	x101
32MB	Not Supported		M25P40	x101
512MB	Not Supported	Chingis (formerly PMC)	Pm25LV512A	x100
1GB	Not Supported		Pm25LV010A	x101
2GB	Not Supported			
4GB	Not Supported			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	0= Advertises the PCI-E device as 2.5GT/s 1= Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCS	Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1:0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 0: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE (Internal PD)	DVPPDATA(23:20)	MEMORY TYPE, MAKE AND SIZE INFO 0000 - GDDR2 64Mx16 500MHz HYNIX 0001 - GDDR2 64Mx16 500MHz SAMSUNG 0010 - Reserve 0011 - Reserve

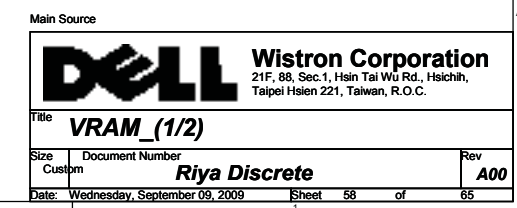
*DEFAULT

Main Source

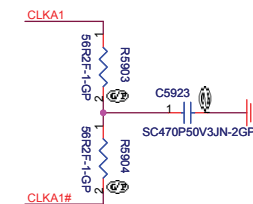
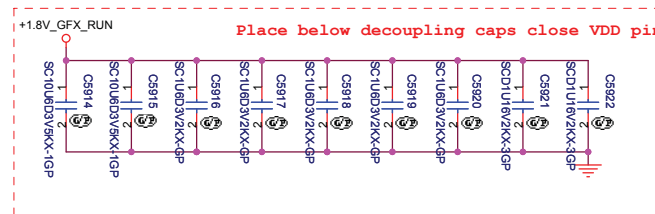
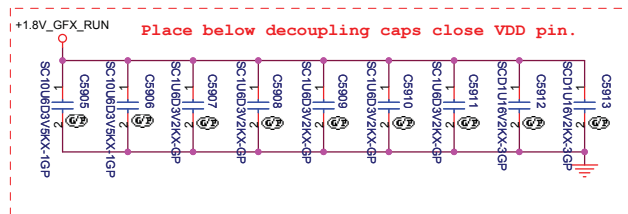
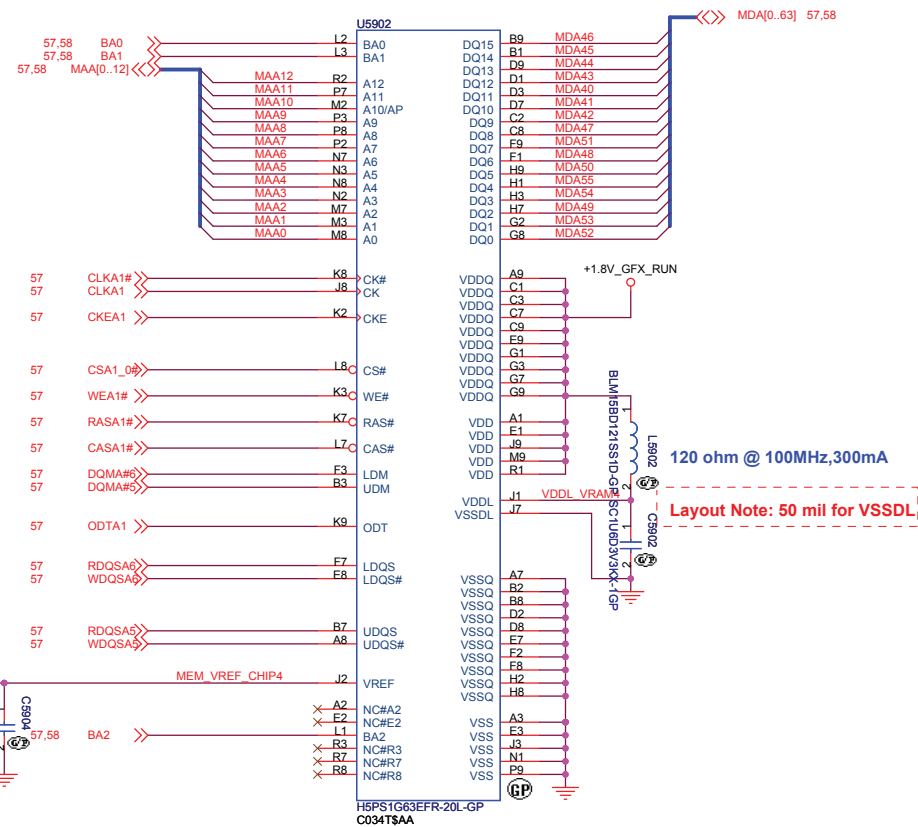
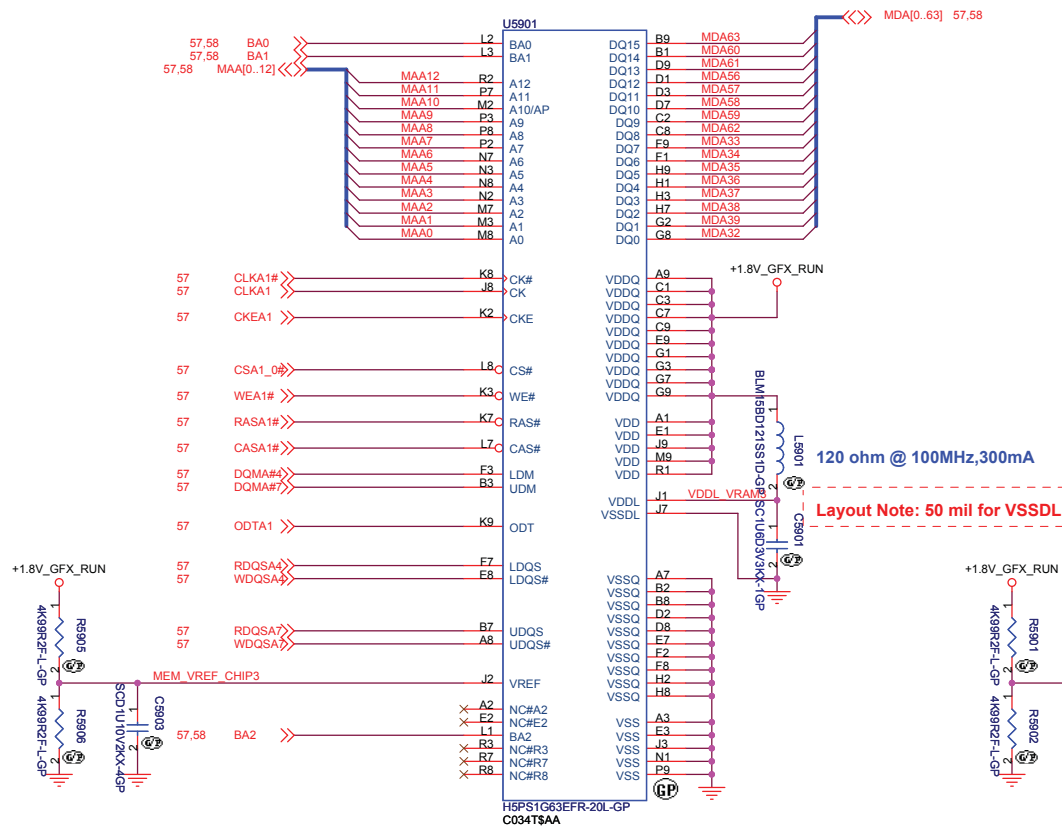


Title	VGA-MEMORY/STRAPS(4/4)	Rev	A00
Size	A2	Document Number	Riya Discrete
Date:	Wednesday, August 26, 2009	Sheet	57 of 65


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1'st 72.51G63.A0U
2'nd 72.41164.G0U
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SSID = VIDEO



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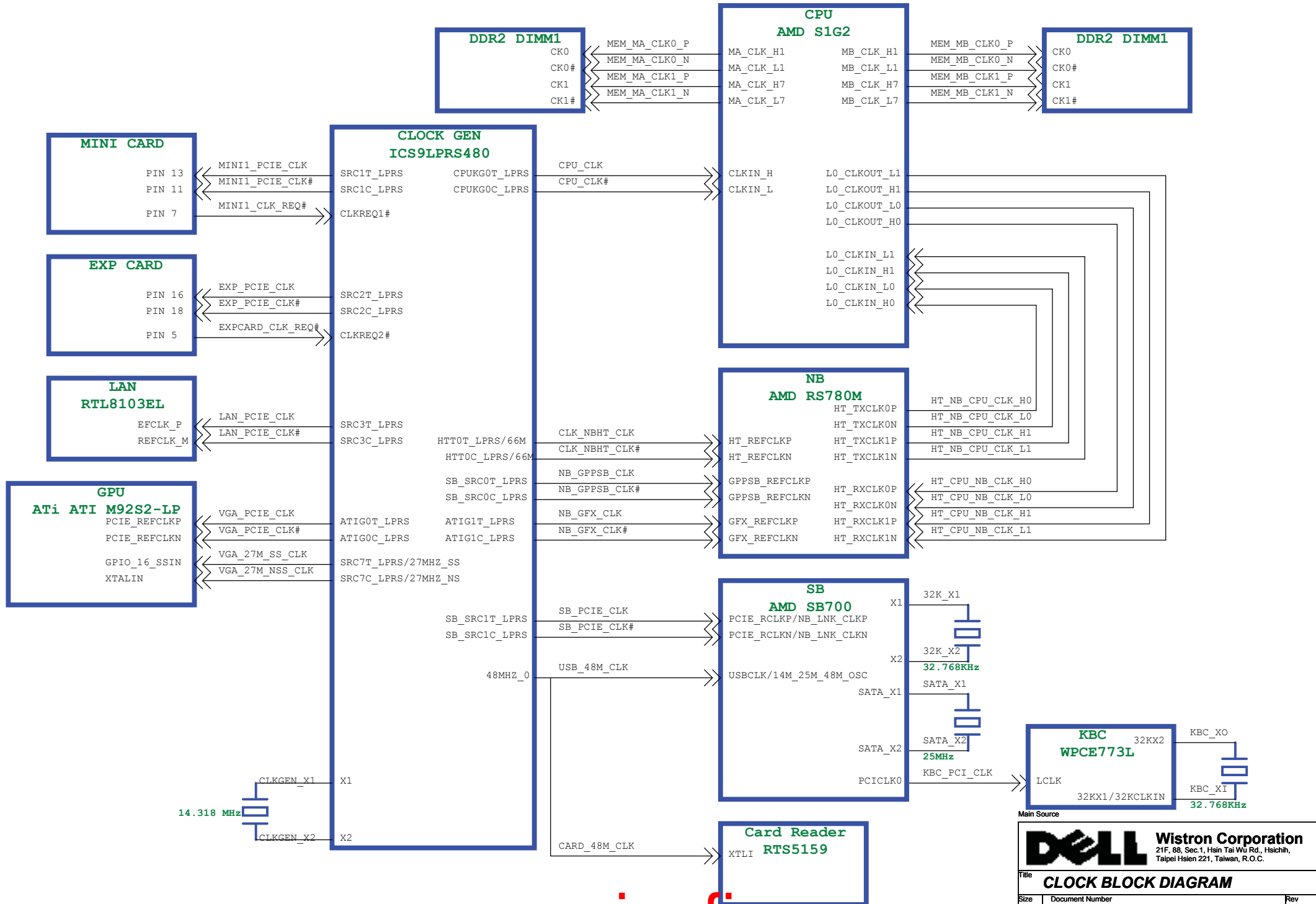
Title	VRAM (2/2)
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Size Custom	Document Number Riya Discrete	Rev A00
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Date: Wednesday, September 09, 2009 Sheet 59 of 65

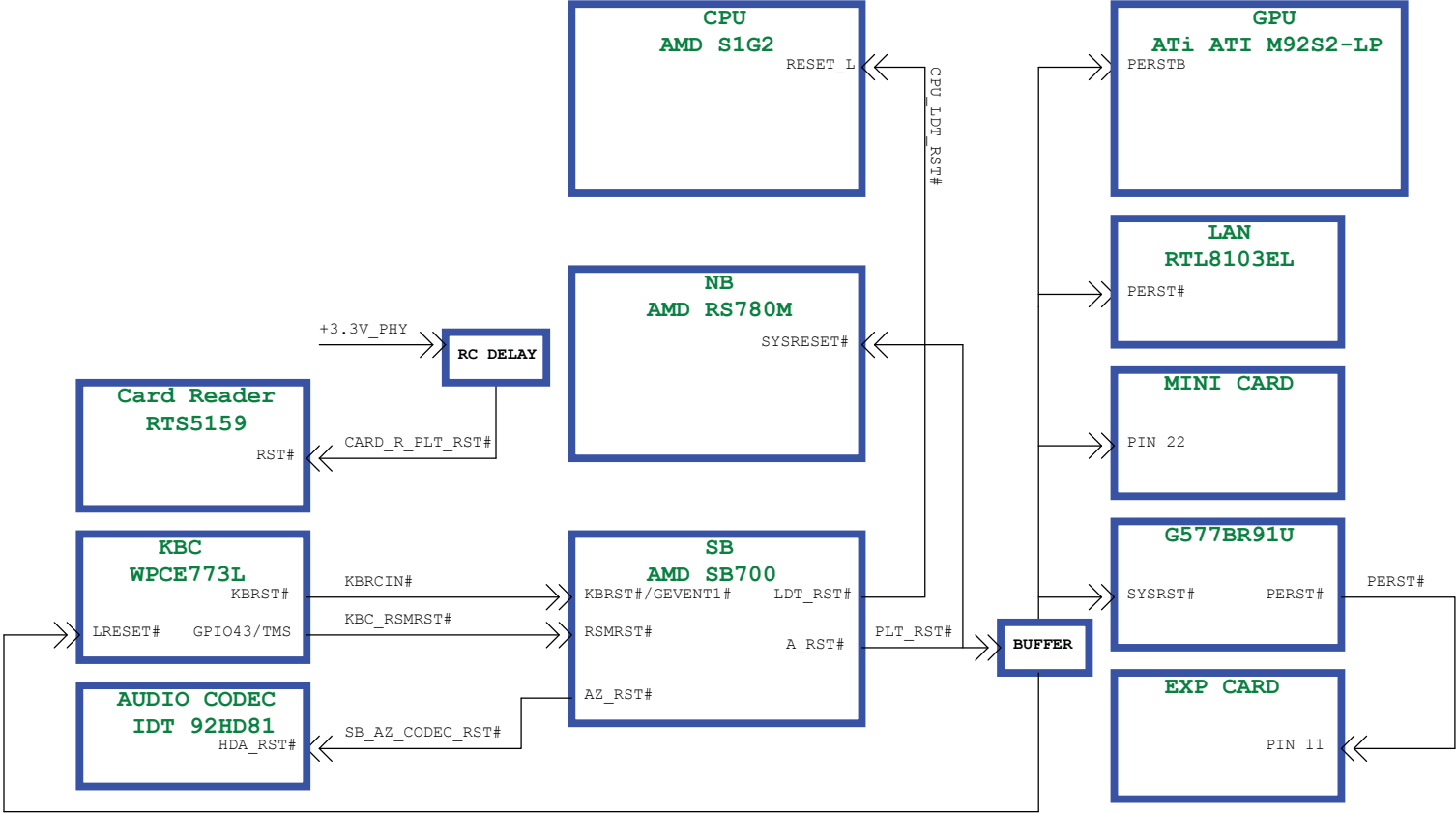
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CLOCK BLOCK DIAGRAM

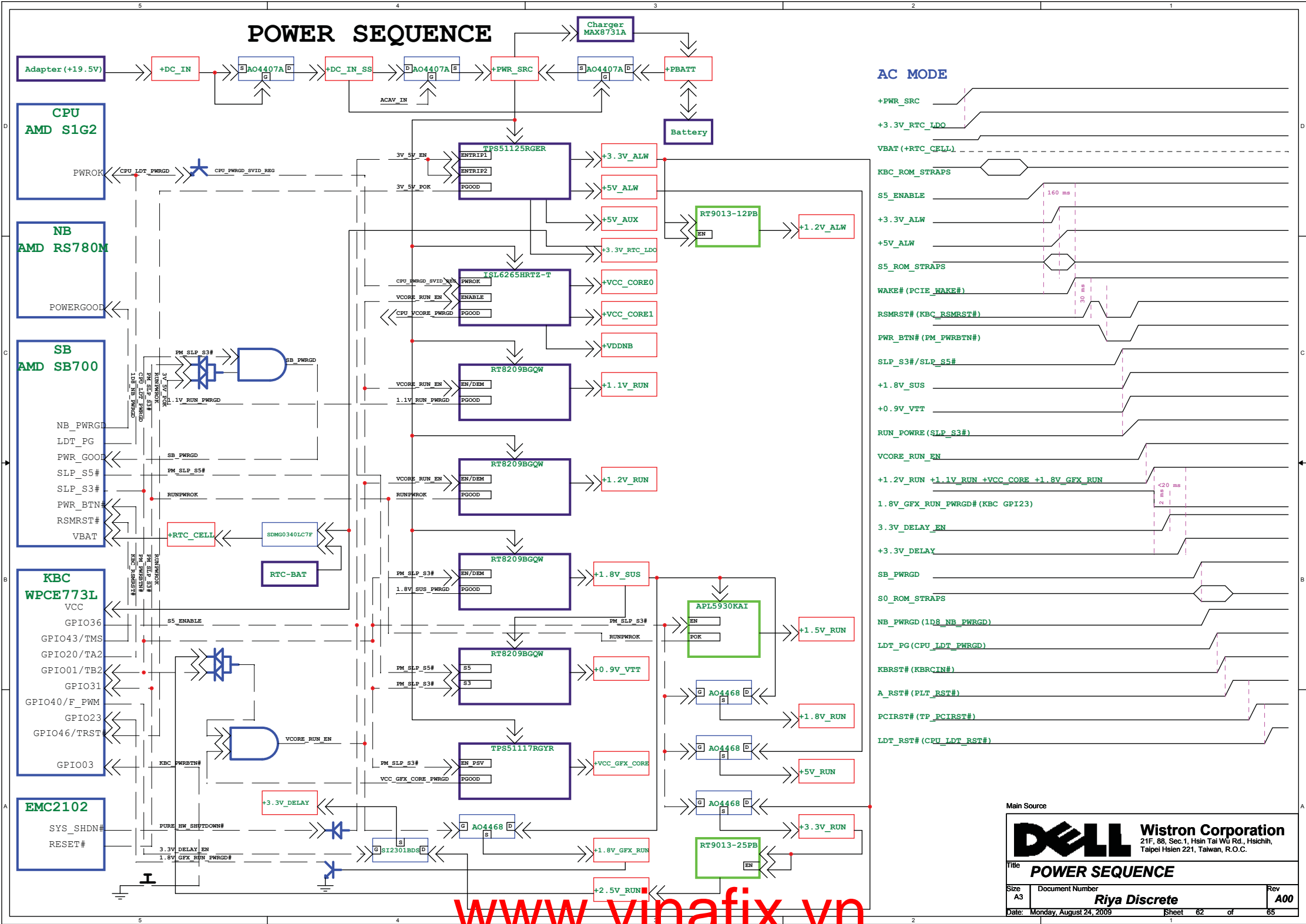


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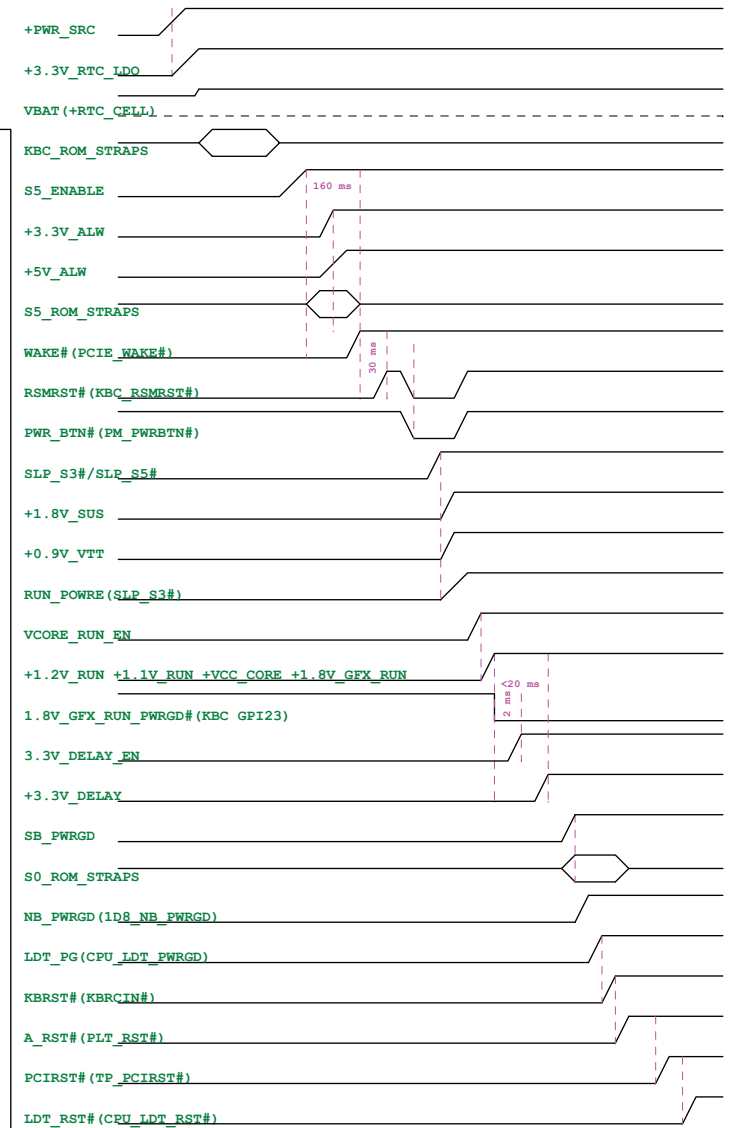
RESET BLOCK DIAGRAM



POWER SEQUENCE



AC MODE



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Title **POWER SEQUENCE**

Size A3	Document Number Riya Discrete	Rev A00
Date: Monday, August 24, 2009	Sheet 62	of 65

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/03/31	X01	1	19	Change DIMM SPD SMBus from Ch1 to Ch0	AGESA by default will look at SMBUS0 for SPD information	EE
		2	49	Use low RDS(on) MOSFET on audio de-pop circuit	Follow DAL's MOSFET to de-pop noise.	EE
		3	19	Change Bluetooth from USB Port-12 to Port-6	Per BIOS request, change bluetooth to port-6	BIOS,EE
		4	39	Change +0.9V_VTT power enable connect with SLP_S5	Per AMD design guideline, VTT should be turn on when S3,so VTT enable signal should tied to SLP_S5#.	EE
		5	20	Add SB GPIO48 To detect LCD Size	Add LCD Size detect Pin	EE
		6	7	Change R709/R710 from 33 ohm to 22 ohm	clock EA test report, vendor recommend change R709/R710 from 33 ohm to 22 ohm.	EE
		7	39	Stuff PR3904 and empty PR3903	Correct BOM errors on schematic	EE
		41		Change PR4103 from 3.3 ohm to 300 ohm		
		39		Stuff PR3910,PR3911		
		41		Stuff PR4105 Dummy PR4106,PC4109	Update schematic base on power on/off fine tune result.	EE
		37		Stuff PR3713 Dummy PR3703		
		31		Stuff R3115 Dummy R3117		
		31		Change R3107 from 200K to 20K ohm		
				Change R3103 from 10K to 0 ohm		
		38		Change R3803 from 0 to 15K ohm		
				Stuff PC3808 to 0.1u		
		9	20	Change SATA HD from Port-3 to Port-0	Per BIOS request, change SATA HD to port-0	EE
		10	19	Change R1914 from 33 Ohm to 47 ohm	Fine tune damping for HD Audio signal EA test result.	EE
		11	26	Change C2611/C2613 from 18P to 15P	Update crystal cap base on x'tal test report	EE
2009/04/06		20		Change C2009/C2010 from 10P to 12P		
		12	27	Add EC GPIO05 To detect LCD Size	Add LCD Size detect Pin	EE
		13	19	Change Clk gen,Mini Card SMBus from Ch1 to Ch0	reduce component quantity , decrease the production cost	EE
		14	18,25	Del R2504,C2510,R1817	Card reader System reset depend on 3.3V_Run power rails, Not reserve for A_RST.	EE
2009/04/08		15	31	Del R3109,R3110,R3111,R3113,R3114,R3116	Not reserve,for try Power Plane Enable.	EE
		16	10,19	Change CPU SID/SIC from SB_SMBus_Ch1 to SCL3_LV/SDA3_LV.	Reduce component quantity , save level shift circuit cost.	EE
		17	57	Stuff R5702	For GPU setting : Full Tx output swing	EE
2009/04/10				Stuff R5703	For GPU setting : Tx de-emphasis enabled	
		18	18	Change C1810/C1812 from 18P to 15P	Update crystal cap base on x'tal test report	EE
		19	27,49	Change netname from HP MUTE to HP MUTE#	This signal is low active, so we need to correct the Netname	EE
2009/04/14		20	29,10	Stuff R2917 Dummy R1022.	SYS_THERMTRIP# By THERMAL IC control	EE
		21	10,15	DEL R1001,R1002,R1003,R1510,R1511	Reduce component quantity , delete 0 ohm ,reserve closed-gap.	EE
2009/04/15		19,27,28		R1902,R2705,R2731,R2905		
		32,42		R3203,R4202,R4203		
		48,55		R4805,R4806,R4809,R5521,R5522		
		22	07	Add EC703 For EMI	This is the solution to solve 999MHz peak issue.	EMI,EE
2009/04/16		23	39	Add R3900,R3901,PQ3900	Use discharge circuit for power on/off.	EE
		24	53	Add C5300,C5301,C5302,C5303,C5304,C5305	Reserve for straddle mot.	EE
2009/04/17		25	15	Del R1508	Not Reserve LDT_RST connect to SYSRESET.	EE
2009/06/09		26	20	Del R2009 R2010		EE
		27	26	stuff C2623 add R2609		EE
		28	27	Del R2736 R2737		EE
		29	27	Connect net LCD_EC_DET to I/O connector		EE
		30	42	Connect LCD1 pin37 to +LCDVDD,Del LCD1 pin38		EE
		31	50	Connect CN5001 pin50 to net LCD_EC_DET,Connect CN5001 pin22 to net +3.3V_RFC_LDO		EE
2009/06/11		32	35	Change PU3501 Ver. from ISL6265HRTZ to ISL6265AHRTZ		EE
2009/06/16		33	23	Change U2301 to new version		EE
		34	42	Change +LCDVDD power solution		EE
2009/06/22		35	29	Empty D2901, Stuff R2902		EE
2009/06/25		36	37,38,39	Change PU3701 PU3801 PU3901 to new version		EE
		37	42	Del D4201 Add R4205		EE

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Title

Change List - EE

Size

A2

Document Number

Riya Discrete

Rev

A00

Date: Monday, August 24, 2009

Sheet

83

of

85

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/08/22	A00	1		change PQ3701,PQ3900,PQ4103,Q3104,Q4202,U2702,U5501 to 84.DMN66.03F	change low level ESD mos to high level material.	Power Team Power Team
		2		Change PQ3301,PQ3302,PQ3303,PQ3304,PQ3401,PQ3402,PQ3403,PQ4101,PQ4104,Q2602,Q2902,Q2903,Q3101,Q3102,Q3103,Q4903,Q5501 to 84.2N702.E31.	change low level ESD mos to high level material.	Power Team Power Team Power Team
		3	42	1.DY R4202, use R4205; 2.change R4202,R4205,R4203 from 0 to 100ohm 3.add R4210,R4211	protect KBC avoid LCD plug-in/out ESD damage.	Power Team Power Team
		4	30	change C3001 from 1uf to 0.1uf.	for sloving CORE_RUN_EN signal shake.	
		5	41	1.DY PWR_CNTL 0 circuit 2.change PR4117,PR4122 to 0 ohm resistor.	change for GFX power control	
		6	27	DY R2720, add R2718	change PCB version	
		7	7	change U701 to 71.08628.003.	change CLK_GEN main source to Selligo	
		8	52	change R5201 from 0 ohm to 100 ohm.	for KBC ESD protect	
		9		change PR3420, PR3506, PR3514,PR3519,PR3529,PR3530,PR3532,PR3534,PR3912,PR3913,PR4004,R1509,R1920,R1921,R2509,R2510,R2724,R5101 from 0 ohm to short pad.	for cost down	
		10	19	Change R1903 from 11.8k to 10.7k	for USB issue	
		11	48	ADD PWR_LED_B AFTE Pad	for AFTE test	
		12		change R701,R702,R704,R1812,R1907,L2003,R2302,R2303,R2304,R2501,R2512,R2508,R2511,R2723,R2902,R3014,R3115,PR3316,PR3713,PR3904,PR4101,PR4105,R4411,R4412,R4901,R4904,R4905,R4906,R4907,R4908 from 0 ohm to short pad.	for cost down	
		13	37	Change PR3712 from 64.10R05.55L to 63.10033.15L Change PR3711 from 64.10025.6DL to 63.10334.1DL	for cost down	
		14		Del L2502,L4401.L4701,L4801	for PSE don't like co-layout	
		15	42	Change EC4202 Pin1 from LCD_TST to LCD_TST_CN		
		16	48	Change R4802,R4807 from 0 ohm to short pad		
		17	49	Change R_USB11_N,R_USB11_P from U4702 Pin3,4 to Pin1,6		
		18	19	Change R1903 from 10K7R2D to 10k7R2F		0903
		19	35	Change PR3520 from 100K to 93.1K Change PR3521 from 18K to 24K	CPU_CORE OCP	0903
		20	41	Change PR4111 from 154K to 52.3K Change PC4112 from 0.047u to 0.1u	VGA_CORE OVP	0903
		21	42	1. Connect LCD1 pin38 to GFX_PWR_SRC 2. Del LCD1 pin37		0903
		22	47	Change R4701,R4702 from 0ohm to short pad		0903
		23		Change RS780 P/N to N131K,SB700 P/N to Y708D		0903
		24	18	Add TP_25M_X1,TP_25M_X2	ATE request	0908
		25	33	Change PC3306,PC3307,PC3314,PC3315 from 78.10622.53L to 78.10622.52L		0908
		26	49	DY Q4903,Q4904,Q4905,Q4906,Q4907.R4911		0908
		27	23	Change U2301 to new version,from 71.92H81.E03 to 71.92H81.G03		0908

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Title Change List - Power			
Size Custom	Document Number Riya Discrete		Rev A00
Date: Wednesday, September 09, 2009	Sheet 65	of	65